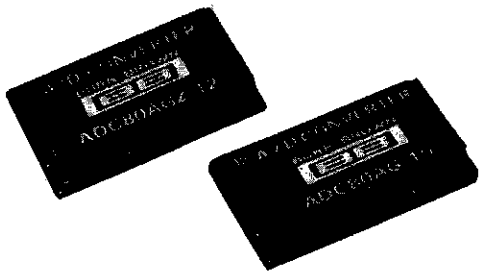
BURR-BROWN®



ADC80

IC ANALOG-TO-DIGITAL CONVERTERS

FEATURES

- **COMPACT DESIGN - Self-contained with internal clock, comparator, and reference**

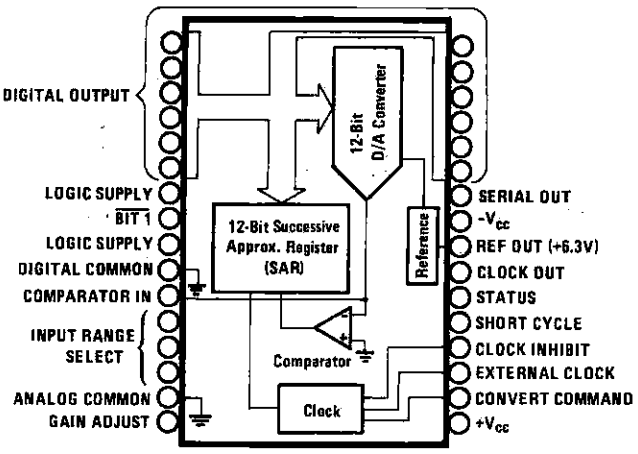
  32-pin ceramic package

- **FAST CONVERSION SPEEDS**
  Provide fast signal sampling rates
  12-bits - 25μsec, 10-bits - 21μsec
  Faster conversion speeds obtainable with "Short-Cycling" and optional external clock

- **LOW COST**

- **WIDE SUPPLY RANGE - Will operate with ±11.4V to ±16V supplies (Z models)**

FUNCTIONAL DIAGRAM



DESCRIPTION

The Model ADC80AG-10 and ADC80AG-12 are 10-and 12-bit successive approximation A/D converters. They utilize state-of-the-art IC and laser-trimmed thin-film components, and are packaged in a compact 32-pin ceramic package.

Complete with internal reference, the ADC80 offers versatility and performance formerly offered only in larger modular or rack-mount packages.

Thin-film internal scaling resistors are provided for the selection of analog input signal ranges of ±2.5V, ±5V, ±10V, 0 to +5V or 0 to +10V.

Gain and offset errors may be externally trimmed to zero, offering initial accuracies of better than ±0.0122% (±1/2LSB). The model ADC80 is specified for -25°C to +85°C operation.

Th fast conversion speeds of 25μsec for 12-bit and 21μsec for 10-bit resolution make the ADC80 excellent for a wide range of applications where system throughput sampling rates from 40kHz to 47kHz are required. In addition, the ADC80 may be short-cycled and an external clock may be used to obtain faster.

Data is available in parallel and serial form with corresponding clock and status signals. All digital input and output signals are DTL/TTL-compatible. Two power supply ranges are available: ±15V and ±12V (Z models). A +5V logic supply is also required.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

PDS-333H

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DISCUSSION OF PERFORMANCE

The accuracy of a successive approximation A/D converter is described by the transfer function shown in Figure 1. All successive approximation A/D converters have an inherent Quantization Error of ±1/2LSB. The remaining errors in the A/D converter are combinations of analog errors due to the linear circuitry, matching, and tracking properties of the ladder and scaling networks, power supply rejection, and reference errors. In summary, these errors consist of initial errors including Gain, Offset, Linearity, Differential Linearity and Power Supply Sensitivity. Initial Gain and Offset errors may be adjusted to zero. Gain drift over temperature rotates the line (Figure 1) about the zero or minus full scale point (all bits OFF) and Offset drift shifts the line left or right over the operating temperature range. Linearity error is unadjustable and is the most meaningful indicator of A/D converter accuracy. Linearity error is the deviation of an actual bit transition from the ideal transition value at any level over the range of the A/D converter. A Differential Linearity error of ±1/2LSB means that the width of each bit step over the range of the A/D converter is 1LSB ±1/2LSB.

The ADC80 is also Monotonic, assuring that the output digital code either increases or remains the same for increasing analog input signals. A monotonic converter

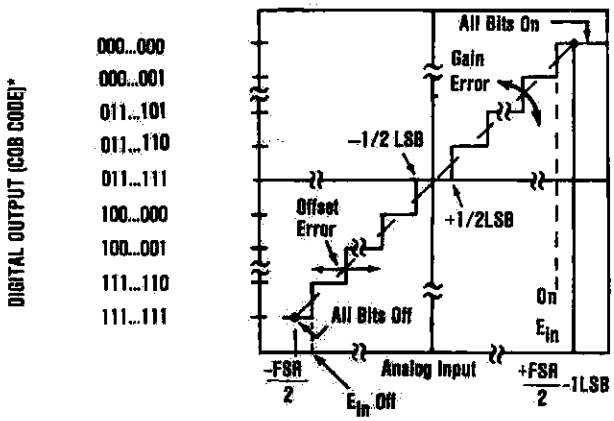


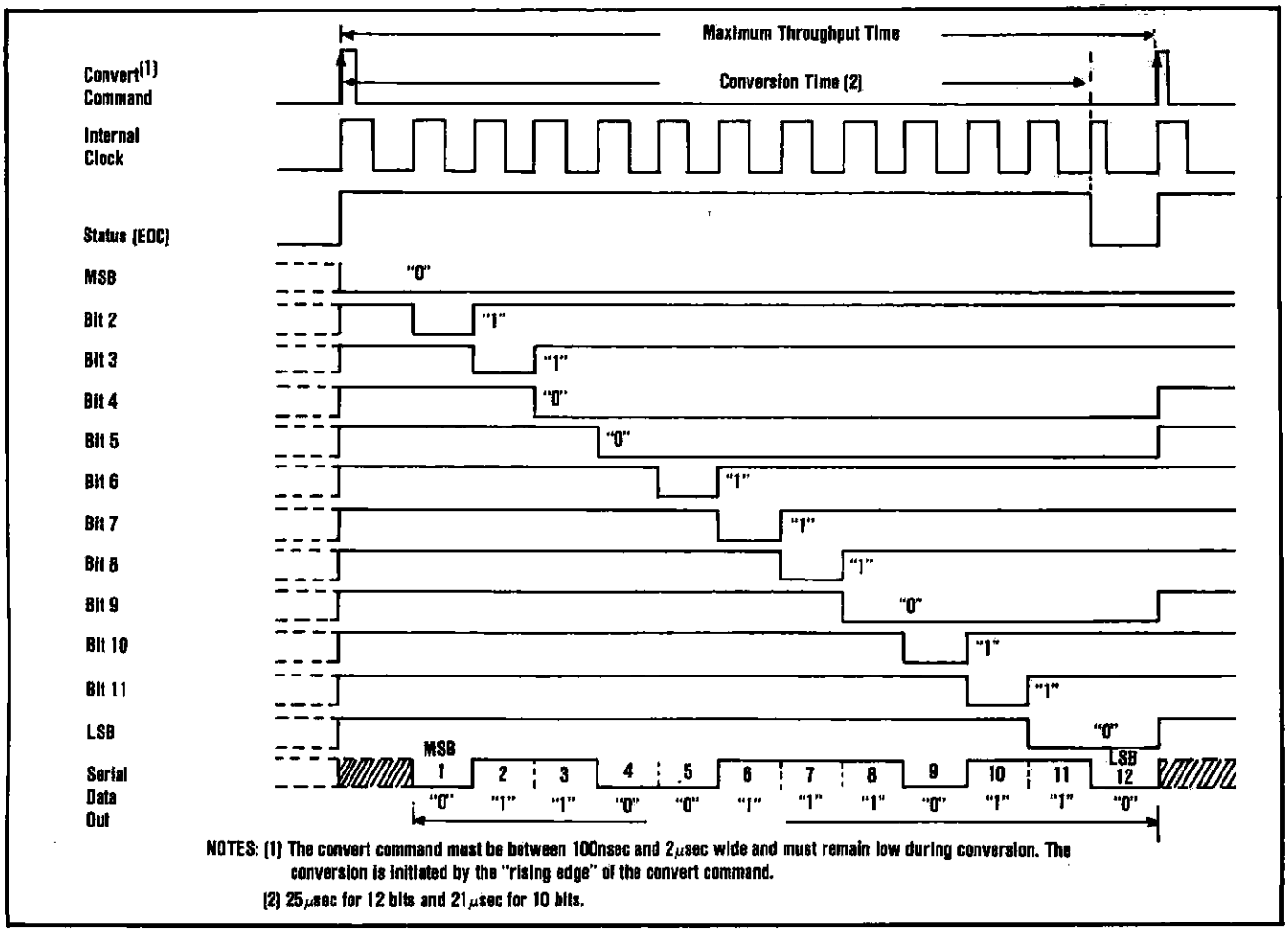
FIGURE 1. Input vs Output for an Ideal Bipolar A/D Converter.

*See Table I for digital code definitions..

can have missing codes; therefore, Burr-Brown specifies no missing codes over a temperature range.

TIMING CONSIDERATIONS

The timing diagram of the ADC80 (Figure 2) assumes an analog input such that the positive true digital word 1001-1000 1001 exists. The output will be complementary as shown in Figure 2 (0110 0111 0110) is the digital output.



NOTES: (1) The convert command must be between 100nsec and 2μsec wide and must remain low during conversion. The conversion is initiated by the "rising edge" of the convert command.
(2) 25μsec for 12 bits and 21μsec for 10 bits.

FIGURE 2. ADC80 Timing Diagram.

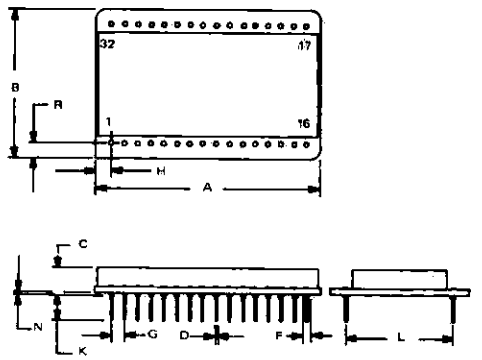
SPECIFICATIONS

ELECTRICAL

Typical at +25°C and rated power supplies unless otherwise noted.

MODEL	ADC80AGZ-12 ADC80AG-12	ADC80AGZ-10 ADC80AG-10	UNITS
RESOLUTION	12	10	Bits
INPUT			
ANALOG INPUTS			
Voltage Ranges - Bipolar	±2.5, ±5, ±10		V
- Unipolar	0 to +5, 0 to +10		V
Impedance (Direct Input)			
0 to +5V, ±2.5V	2.5		kΩ
0 to +10V, ±5V	5		kΩ
±10V	10		kΩ
DIGITAL INPUTS(1)			
Convert Command	Positive Pulse 100nsec Wide (min) 2μsec Wide (max).		
Logic Loading	1		TTL Load
External Clock	1		TTL Load
TRANSFER CHARACTERISTICS			
ERROR			
Gain Error(2)	±0.1		%
Offset Error(2) - Unipolar	±0.05		% of FSR(3)
- Bipolar	±0.1		% of FSR
Linearity Error, max(4)	±0.012	±0.048	% of FSR
Inherent Quantization Error	±1/2		LSB
Differential Linearity Error	±1/2		LSB
No Missing Codes Temp. Range	0 to +70	0 to +70	°C
Power Supply Sensitivity			
±15V	±0.0030		% of FSR/%V_S
+5V	±0.0015		% of FSR/%V_S
DRIFT			
Specification Temperature Range	-25 to +85		°C
Total Accuracy, Bipolar, max(5)	±23		ppm/°C
Gain, max	±30		ppm/°C
Offset - Unipolar	±3		ppm of FSR/°C
Bipolar, max	±15		ppm of FSR/°C
Linearity, max	±3		ppm of FSR/°C
Monotonicity	GUARANTEED		
CONVERSION SPEED(max)(6)	25	22	μsec
OUTPUT			
DIGITAL DATA (all codes complementary)			
Parallel			
Output Codes(7) - Unipolar	CSB		
- Bipolar	COB, CTC		
Output Drive	2		TTL Loads
Serial Data Codes (NRZ)	CSB, COB		
Output Drive	2		TTL Loads
Status	Logic "1" during conversion		
Status Output Drive	2		TTL Loads
Internal Clock			
Clock Output Drive	2		TTL Loads
Frequency(8)	500		kHz
INTERNAL REF. VOLTAGE	6.3		V
Max. External Current (with no degradation of specifications)	200		μA
Tempco of Drift, max	±20		ppm/°C
POWER REQUIREMENTS			
Rated Voltages	±15, +5		V
Z models	±12, +5		V
Range for Rated Accuracy	4.75 to 5.25 and ±14.0 to ±16.0		V
Z models	4.75 to 5.25 and ±11.4 to ±16.0		V
Supply Drain +15V or +12V	+20		mA
-15V or -12V	-20		mA
+5V	+70		mA
TEMPERATURE RANGE			
Specification	-25 to +85		°C
Operating (derated spec)	-55 to +100		°C
Storage	-55 to +125		°C

MECHANICAL



NOTE: LEADS IN TRUE POSITION WITHIN .010" (.25mm) R @ MMC AT SEATING PLANE.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.700	1.760	43.18	44.70
B	1.120	1.160	28.45	29.46
C	.170	.230	4.32	5.84
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.900 BASIC		22.86 BASIC	
N	.002	.010	0.05	0.25
R	.110	.130	2.79	3.30

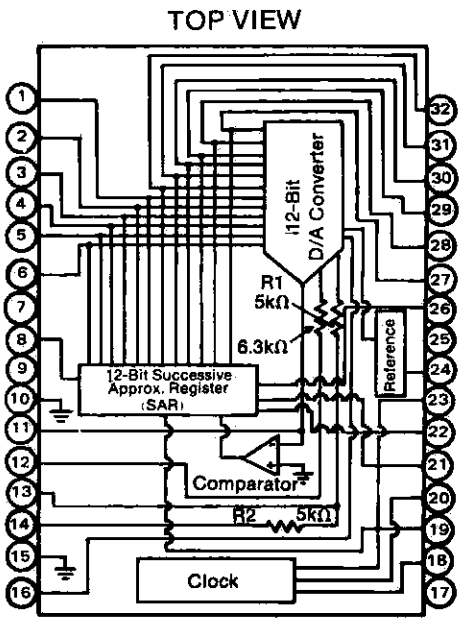
CASE: Ceramic
MATING CONNECTOR: 2302MC - Set of two 16-pin strips $9.40 per set.
WEIGHT: 13 grams (0.46oz.)

1. DTL/TTL compatible, i.e., Logic "0" = 0.8V max, Logic "1" = 2.0V min for inputs and for digital outputs, Logic "0" = +0.4V max and "1" = 2.4V min.
2. Adjustable to zero with external trimpots.
3. FSR means Full Scale Range - for example, unit connected for ±10V range has 20V FSR.
4. Error shown is the same as ±1/2LSB max for resolution of A/D converter.
5. Includes drift due to linearity, gain, and offset drifts.
6. Conversion time with internal clock.
7. See Table I. CSB - Complementary Straight Binary.
   COB - Complementary Offset Binary.
   CTC - Complementary Two's Complement.
8. For conversion speeds specified.

CONNECTION DIAGRAM

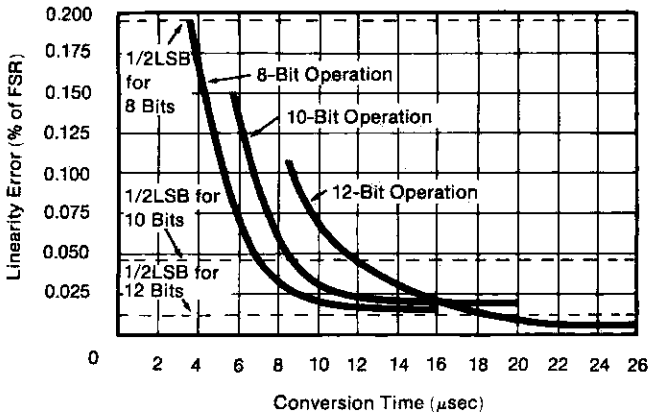
Pin 1 - BIT 6
Pin 2 - BIT 5
Pin 3 - BIT 4
Pin 4 - BIT 3
Pin 5 - BIT 2
Pin 6 - BIT 1 (MSB)
Pin 7 - +5V ANALOG SUPPLY
Pin 8 - $\overline{\text{BIT 1 (MSB)}}$
Pin 9 - +5V DIGITAL SUPPLY
Pin 10 - DIGITAL COMMON
Pin 11 - COMPARATOR IN
Pin 12 - BIPOLAR OFFSET
Pin 13 - R1 10V RANGE
Pin 14 - R2 20V RANGE
Pin 15 - ANALOG COMMON
Pin 16 - GAIN ADJUST

Pin 32 - BIT 7
Pin 31 - BIT 8
Pin 30 - BIT 9
Pin 29 - BIT 10 (LSB-10 BITS)
Pin 28 - BIT 11
Pin 27 - BIT 12 (LSB-12 BITS)
Pin 26 - SERIAL OUT
Pin 25 - -15V OR -12V (Z MODELS)
Pin 24 - REF. OUT (+6.3V)
Pin 23 - CLOCK OUT
Pin 22 - STATUS
Pin 21 - SHORT CYCLE
Pin 20 - CLOCK INHIBIT
Pin 19 - EXTERNAL CLOCK
Pin 18 - CONVERT COMMAND
Pin 17 - +15V or +12V (Z MODELS)

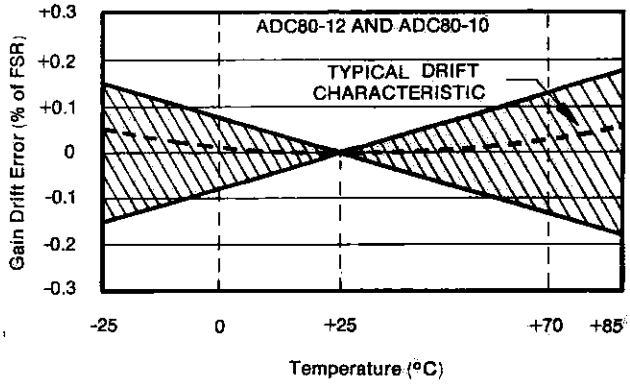


TYPICAL PERFORMANCE CURVES

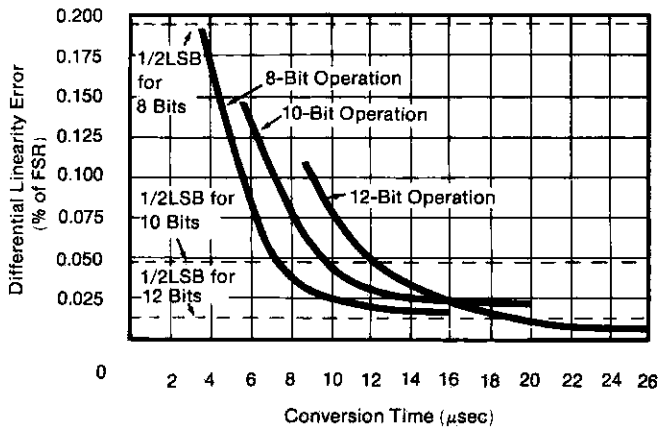
LINEARITY ERROR VS CONVERSION TIME



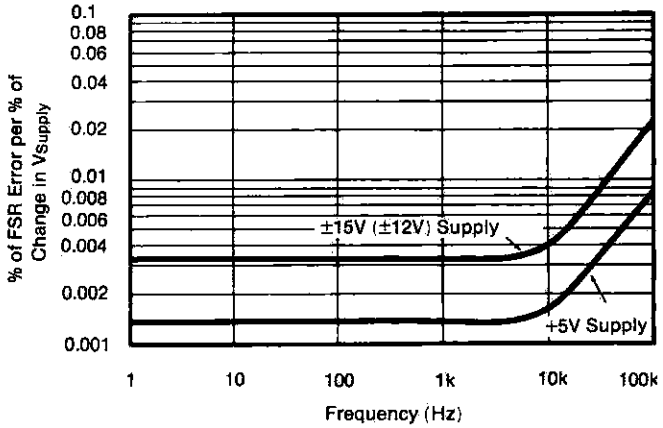
GAIN DRIFT ERROR VS TEMPERATURE



DIFFERENTIAL LINEARITY ERROR VS CONVERSION TIME



POWER SUPPLY REJECTION VS POWER SUPPLY RIPPLE FREQUENCY



DEFINITION OF DIGITAL CODES

PARALLEL DATA

Three binary codes are available on the ADC80 parallel output; they are complementary (logic "0" is true) straight binary (CSB) for unipolar input signal ranges and complementary two's complement (CTC) and complementary offset binary (COB) for bipolar input signal ranges.

Table I describes the LSB, transition values and code definitions for each possible ADC80 analog input signal range.

SERIAL DATA

Two straight binary (complementary) codes are available on the serial output line of the ADC80; they are CSB and COB. The serial data is available only during conversion and appears with the most significant bit (MSB) occurring first. The serial data is synchronous with the internal clock as shown in the timing diagram of Figure 2. The LSB and transition values shown in Table I also apply to the serial data output except for the CTC code.

TABLE I. Input Voltages, Transition Values, LSB Values, and Code Definitions.

Binary (BIN) Output	INPUT VOLTAGE RANGE AND LSB VALUES					
Analog Input Voltage Range	Defined As:	±10V	+5V	±2.5V	0 to +10V	0 to +5V
Code Designation		COB or CTC*	COB or CTC*	COB or CTC*	CSB**	CSB**
One Least Significant Bit (LSB)	$\frac{FSR}{2^n}$	$\frac{20V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$	$\frac{10V}{2^n}$	$\frac{5V}{2^n}$
	n = 8	78.13mV	39.06mV	19.53mV	39.06mV	19.53mV
	n = 10	19.53mV	9.77mV	4.88mV	9.77mV	4.88mV
	n = 12	4.88mV	2.44mV	1.22mV	2.44mV	1.22mV
Transition Values MSB LSB						
000...000***	+Full Scale	+10V-3/2LSB	+5V -3/2LSB	+2.5V -3/2LSB	+10V -3/2LSB	+5V -3/2LSB
011...111	Mid Scale	0	0	0	+5V	+2.5V
111...110	-Full Scale	-10V +½LSB	-5V +½LSB	-2.5V +½LSB	0 + ½LSB	0 +½LSB

* COB = Complementary Offset Binary
** CSB = Complementary Straight Binary
*CTC = Complementary Two's Complement - obtained by using the complement of the most significant bit ($\overline{MSB}$). $\overline{MSB}$ is available on pin 8.
*** Voltages given are the nominal value for transition to the code specified.

DISCUSSION OF SPECIFICATIONS

The ADC80 is specified to provide critical performance criteria for a wide variety of applications. The most critical specifications for an A/D converter are linearity, drift, gain and offset errors and conversion speed effects on accuracy. The ADC80 is factory-trimmed and tested for all critical key specifications.

GAIN AND OFFSET ERROR

Initial Gain and Offset errors are factory-trimmed to ±0.1% of FSR (±0.05% for unipolar offset) at 25°C. These errors may be trimmed to zero by connecting external trim potentiometers as shown on next page.

ACCURACY DRIFT VS TEMPERATURE

Three major drift parameters degrade A/D converter accuracy over temperature; they are gain, offset and linearity drift. The worst case accuracy drift is the summation of all three drift errors over temperature. Statistically, these errors do not add algebraically, but are random variables which behave as root-sum-squared (RSS) or 1δ errors as follows:

$$RSS = \sqrt{\epsilon g^2 + \epsilon o^2 + \epsilon e^2}$$

where ϵg = gain drift error (ppm/°C)
ϵo = offset drift error (ppm of FSR/°C)
ϵe = linearity error (ppm of FSR/°C)

For unipolar operation, the total RSS drift is ±30.3ppm/°C.

ACCURACY VS SPEED

In successive approximation A/D converters, the conversion speed affects linearity and differential linearity errors. Conversion speed and its effect on linearity and differential linearity errors for the ADC80 are shown in Typical Performance Curves.

The ADC80 conversion speeds are specified for a maximum linearity error of ±1/2LSB and a differential linearity error of ±1/2LSB with the internal clock. Faster conversion speeds up to 23μsec for 12 bits, 12μsec for 10 bits and 6μsec for 8 bits are possible with an external clock.

POWER SUPPLY SENSITIVITY

Changes in the DC power supplies will affect the accuracy of the ADC80. The ADC80 power supply sensitivity is specified for ±0.003% of FSR/%V_S for ±15V (±12V) supplied for ±0.0015% of FSR/%V_S for +5V supplies. Normally, regulated power supplies with 1% or less ripple are recommended for use with the ADC80. See layout precautions and power supply decoupling on next page.

LAYOUT AND OPERATING INSTRUCTIONS

LAYOUT PRECAUTIONS

Analog and digital commons are not connected internally in the ADC80 but should be connected together as close to the unit as possible, preferably to a large ground plane under the ADC80. If these grounds must be run separately, use wide conductor pattern and a 0.01μF to 0.1μF nonpolarized bypass capacitor between analog and digital commons at the unit. Low impedance analog and digital common returns are essential for low noise performance. Coupling between analog input and digital lines should be minimized by careful layout. Analog and digital +5V supplies are also not connected internally; they should be connected together at the unit as shown below in Figure 3 (Pins 7 and 9).

POWER SUPPLY DECOUPLING

The power supplies should be bypassed with tantalum or electrolytic type capacitors as shown in Figure 3 to obtain noise free operation. These capacitors should be located close to the ADC80. 1μF electrolytic type capacitors should be bypassed with 0.01μF ceramic capacitors for improved high frequency performance.

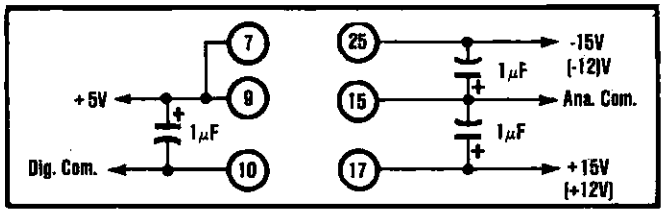


FIGURE 3. Recommended Power Supply Decoupling.

OPTIONAL EXTERNAL GAIN AND OFFSET ADJUSTMENTS

Gain and Offset errors may be trimmed to zero using external gain and offset trim potentiometers connected to the ADC80 as shown in Figures 5 and 6. Multiturn potentiometers with 100ppm/°C or better TCR's are recommended for maximum drift over temperature and time. These pots may be any value from 10kΩ to 100kΩ. All resistors should be 20% carbon or better. Pin 16 (Gain Adjust) may be left open if no external adjustment is required.

ADJUSTMENT PROCEDURE

OFFSET - Connect the Offset potentiometer as shown in Figure 5. Sweep the input through the end point transition voltage that should cause an output transition to all ones.

Adjust the Offset potentiometer until the actual end point transition voltage occurs at E_{IN}^{OFF}. The ideal transition voltage values of the input are given in Table I.

GAIN - Connect the Gain adjust potentiometer as shown in Figure 6. Sweep the input through the end point transition voltage that should cause an output transition to all zeros.

Adjust the Gain potentiometer until the actual end point transition voltage occurs at E_{IN}^{ON}.

Table I details the transition voltage levels required.

INPUT SCALING

The ADC80 input should be scaled as close to the maximum input signal range as possible in order to utilize the maximum signal resolution of the A/D converter. Connect the input signal as shown in Table II. See Figure 4 for circuit details.

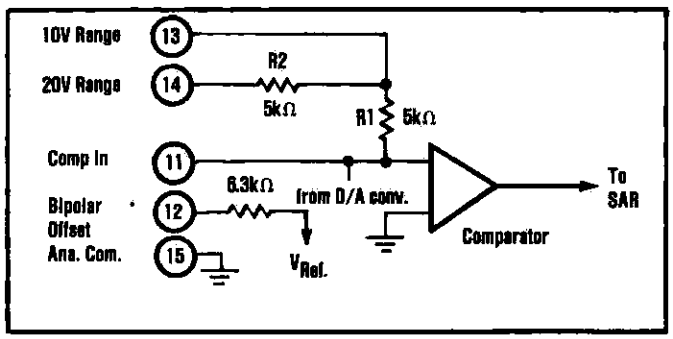


FIGURE 4. ADC80 Input Scaling Circuit.

TABLE II. ADC80 Input Scaling Connections.

Input Signal Range	Output Code	Connect Pin 12 To Pin	Connect Pin 14 To	Connect Input Signal To
±10V	COB or CTC	11	Input Signal	14
±5V	COB or CTC	11	Open	13
±2.5V	COB or CTC	11	Pin 11	13
0 to +5V	CSB	15	Pin 11	13
0 to +10V	CSB	15	Open	13

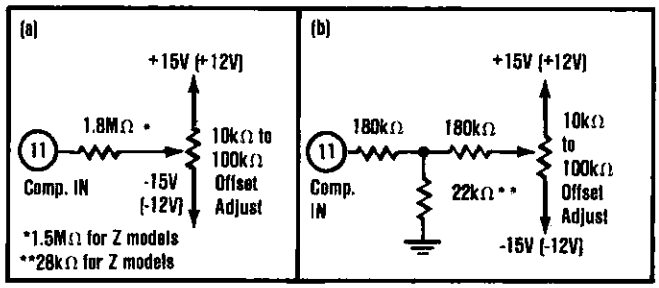


FIGURE 5. Two Methods of Connecting Optional Offset Adjust with a 0.4% of FSR Range Adjustment.

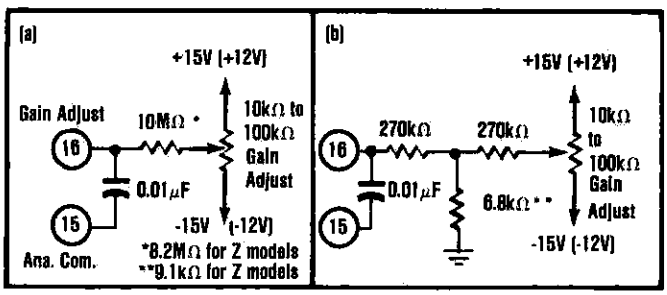


FIGURE 6. Two Methods of Connecting Optional Gain Adjust with a 0.6% Range of Adjustment.

CLOCK OPTIONS

The ADC80 is extremely versatile in that it can be operated in several different modes with either internal or external clock. Most of these options can be implemented with nothing more than an inexpensive quad 2-input NAND gate (7400) as shown in Figures 7 through 10.

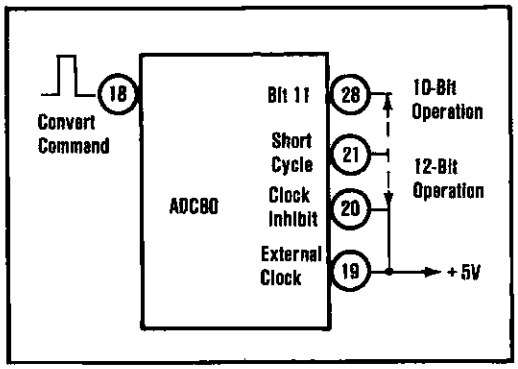


FIGURE 7. Internal Clock - Normal Operating Mode. (Conversion initiated by the rising edge of the convert command. The internal clock runs only during conversion.)

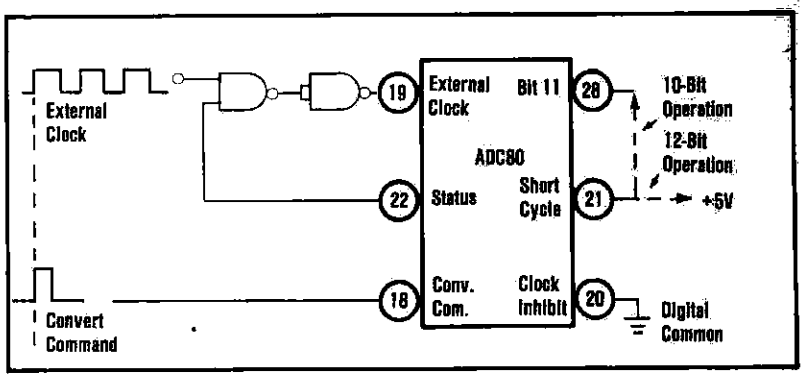


FIGURE 9. Continuous External Clock. (Conversion initiated by rising edge of convert command. The convert command must be synchronized with clock.)

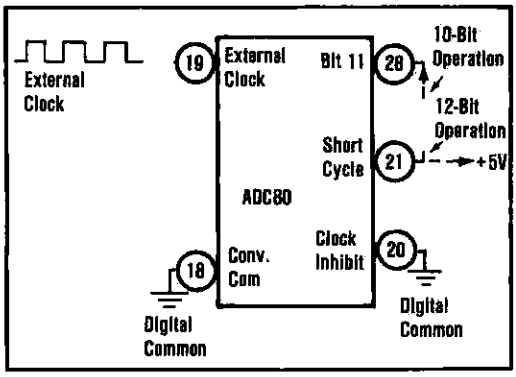


FIGURE 8. Continuous Conversion with External Clock. (Conversion is initiated by 14th clock pulse. Clock runs continuously.)

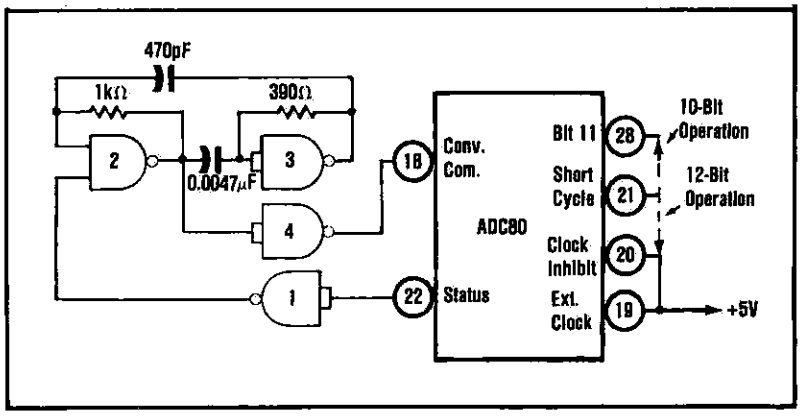


FIGURE 10. Continuous Conversion with Internal Clock. (Conversion is initiated by the 14th clock pulse. Clock runs continuously. The oscillator formed by gates 2 and 3 insures that the conversion process will start when logic power is first turned on.)

SHORT CYCLE FEATURE

The ADC80 may be operated at faster speeds for resolutions less than 10 or 12 bits, depending on the model selected, by connecting the short cycle pin, pin 21, as shown in Table III. Conversion speeds, linearity, and resolutions are shown for reference.

TABLE III. Short Cycle Connections and Resolutions for 8- to 12-bit Resolutions - ADC80.

RESOLUTION (BITS)	12	10	8
Connect Pin 21 to	Pin 9	Pin 28	Pin 30
Maximum Conversion Time[1]			
Internal Clock (μsec)	25	22	18
External Clock (μsec)	23	12	6
Maximum Nonlinearity At +25°C (% of FSR)	0.012[2]	0.048[3]	0.20[3]

NOTES: (1) Max conversion time to maintain ±½LSB Nonlinearity error.
(2) 12 Bit Models only.
(3) 10 or 12 Bit Models.

OUTPUT DRIVE

Normally all ADC80 logic outputs will drive 2 standard TTL loads; however, if long digital lines must be driven, external logic buffers are recommended.

APPLICATIONS

LOW COST DATA ACQUISITION SYSTEM

When combined with a sample/hold, multiplexer and simplified logic, a 16-channel 12-bit, 25kHz data acquisition system can be built for less than $125.00 parts cost.

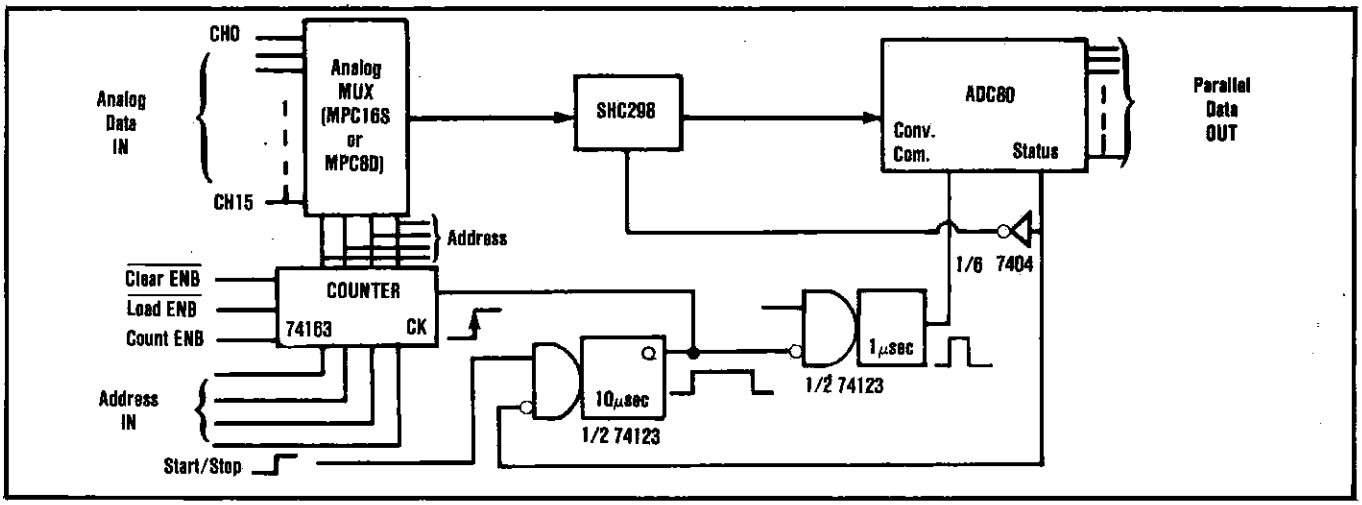


FIGURE 11. Low Cost Data Acquisition System.

ZERO DROOP SAMPLE/HOLD

A zero droop - infinite hold sample/hold can be constructed with the ADC80 with the circuit shown in Figure 12. A sample command will cause the relay to switch the analog input to the ADC80 input and also generate a convert command to the ADC80. The sample pulse width (T_A) should be greater than the combined switching and settling time of the relay and driver circuit and the ADC80 conversion time.

In the Hold mode, the analog value can be held indefinitely with zero droop. The period of the first one-shot multivibrator must be equal to or greater than T_R, the switching time of the relay.

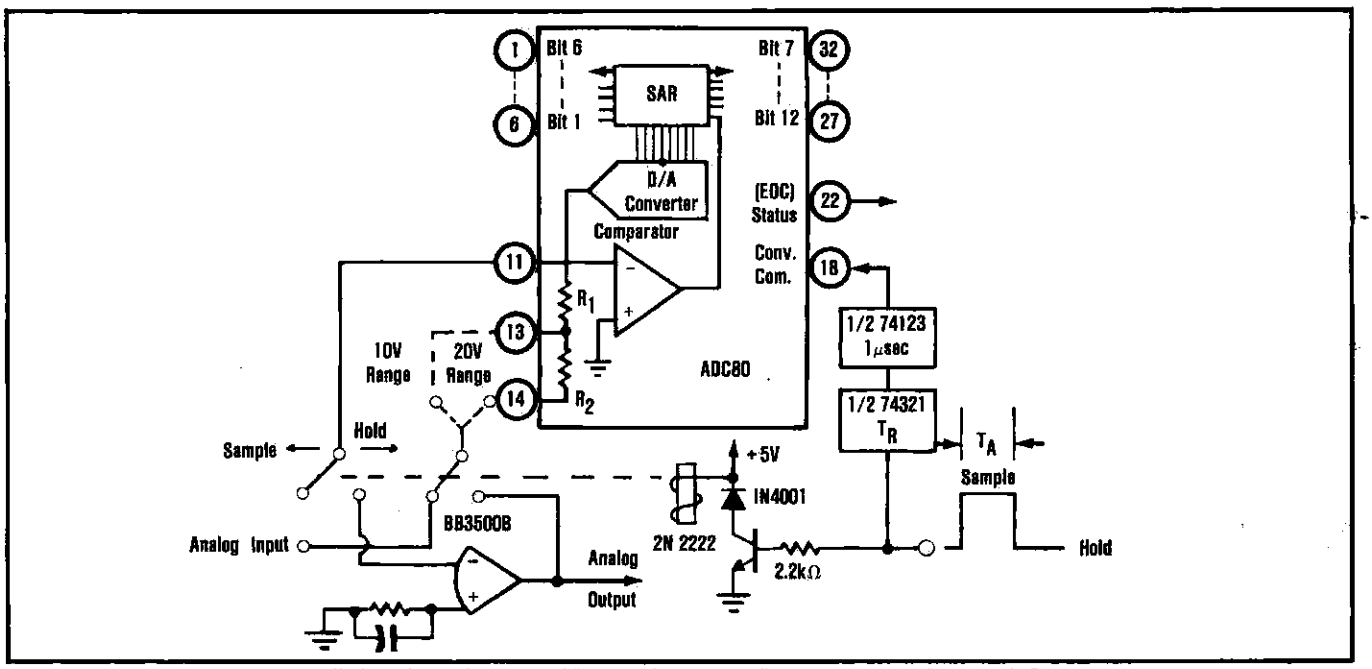


FIGURE 12. Zero Droop Infinite Hold Sample/Hold using ADC80 and a Few External Components.

ORDERING INFORMATION

ADC80AG - XX

A/D Converter family	Blank - ±14.0V to ±16.0V Supply range	Resolution (No. of Bits)
A = -25°C to +85°C	Z - ±11.4V to ±16.0V supply range	10 = 10 Bits
G = Ceramic Package		12 = 12 Bits

BURR-BROWN®

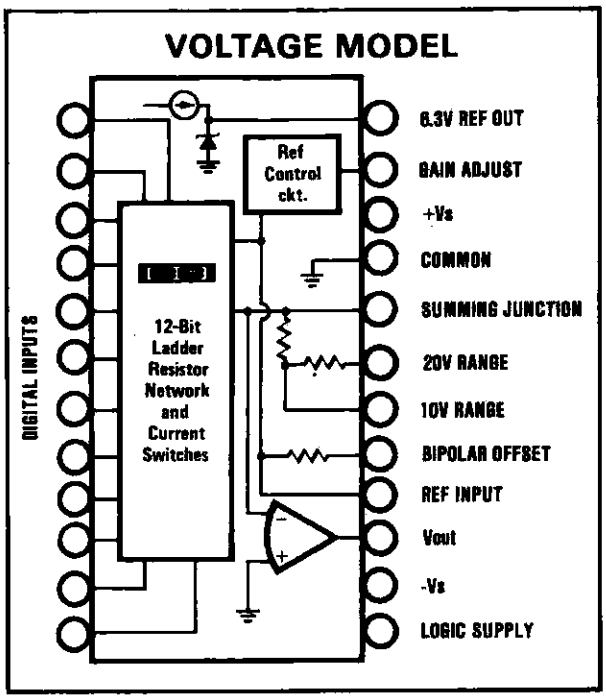
DAC80

RECEIVED NOV 9 1984

Integrated Circuit DIGITAL-TO-ANALOG CONVERTER

FEATURES:

- WIDE POWER SUPPLY RANGE MODELS AVAILABLE (Z MODELS)
- 12-BIT, 3-DIGIT RESOLUTION
- ±1/2LSB MAXIMUM NONLINEARITY
- COMPLETE WITH INTERNAL REFERENCE AND OUTPUT AMPLIFIER (V MODELS)
- FAST SETTLING - 300nsec to ±0.01% (I MODELS)
- CERAMIC DUAL-IN-LINE PACKAGE
- LOW COST



DESCRIPTION

Use this popular 12-bit digital-to-analog converter for low cost precision performance applications.

DAC80, with internal reference and optional output amplifier, offers a maximum nonlinearity error of ±0.012%, ±30ppm/°C maximum gain drift, and monotonicity - all over a 0°C to 70°C operating range. In the bipolar configuration, total accuracy drift is guaranteed to be less than ±25ppm/°C. Select TTL compatible complementary 12-bit binary (CBI) or 3-digit BCD (CCD) input codes.

Packaged within DAC80's 24-pin dual-in-line ceramic case are fast-settling switches and stable, laser-trimmed thin-film resistors that let you select output voltage ranges of ±2.5, ±5, ±10, 0 to +5, 0 to +10 volts (V models) or output current ranges of ±1mA or 0 to -2mA (I models). Voltage output models settle to ±0.01% of FSR in 3μsec for a 10V step change.

By specifying the new DAC80Z model with a supply range of ±11.4V to ±16.0V, you can use this proven D/A converter in microprocessor and semiconductor memory systems.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

Printed in U.S.A. March, 1984

SPECIFICATIONS

Typical at 25°C and rated power supplies unless otherwise noted.

ELECTRICAL

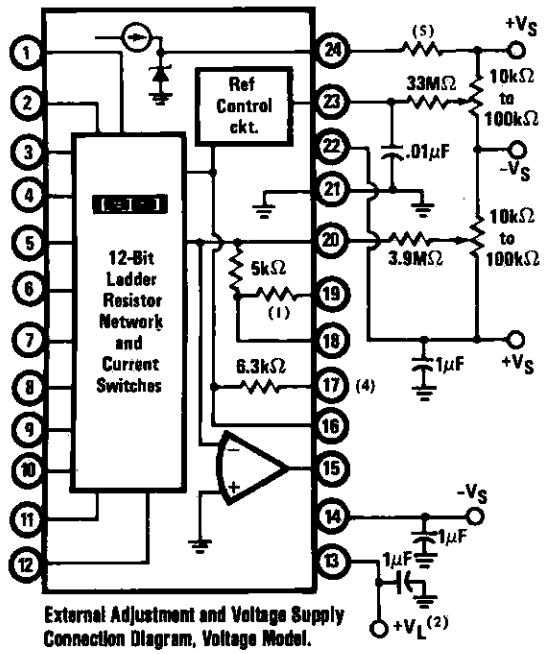
MODEL	DAC80CBI			DAC80CCD			
	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
DIGITAL INPUT							
Resolution			12				Bits
						3	Digits
Logic Levels (TTL/Compatible)(1)							
Logic "1" (+40μA max at +5.0V)	+2.4		+5.0	+2.4		+5.0	VDC
Logic "0" (1.6mA max at +0.4V)	0		+0.4	0		+0.4	VDC
ACCURACY							
Linearity Error at 25°C		±1/4	±1/2		±1/8	±1/4	LSB
Differential Linearity Error		±1/2	+1, -3/4		±1/4	±1/2	LSB
Gain Error(2)		±0.1	±0.3		±0.1	±0.3	%
Offset Error(2)		±0.05	±0.15		±0.05	±0.15	% of FSR(3)
Monotonicity Temp. Range, min	0		+70	0		+70	°C
DRIFT(4) (0°C to +70°C)							
Total bipolar drift, max (includes gain, offset, and linearity drifts)(5)			±25			±25	ppm of FSR/°C
Total error over 0°C to +70°C(6)							
Unipolar		±0.08	±0.15		±0.08	±0.15	% of FSR
Bipolar		±0.06	±0.12		±0.06	±0.12	% of FSR
Gain		±15	±30		±15	±30	ppm/°C
Exclusive of internal reference			±10			±10	ppm/°C
Unipolar Offset		±1	±3		±1	±3	ppm of FSR/°C
Bipolar Offset		±7	±15		±7	±15	ppm of FSR/°C
Differential Linearity 0°C to +70°C		±1/2	+1, -7/8		±1/2	+1, -7/8	LSB
Linearity Error 0°C to +70°C			±1/2			±1/2	LSB
CONVERSION SPEED/V models							
Settling Time to ±0.01% of FSR For FSR Change							
with 10kΩ Feedback		5			5		μsec
with 5kΩ Feedback		3			3		μsec
For 1LSB Change		1.5			1.5		μsec
Slew Rate	10	20		10	20		V/μsec
CONVERSION SPEED/I models - of FSR							
Settling Time to ±0.01% For FSR Change							
10Ω to 100Ω Load		300			300		nsec
1kΩ Load		1			1		μsec
ANALOG OUTPUT/V models							
Ranges(7)	±2.5, ±5, ±10, 0 to +5, 0 to +10				0 to +10		Volts
Output Current	±5			±5			mV
Output Impedance (DC)		0.05			0.05		ohms
Short Circuit Duration	Indefinite to Common						
ANALOG OUTPUT/I models							
Ranges		±1, 0 to -2			0 to -2		mA
Output Impedance - Bipolar		4.4			4.4		kΩ
Output Impedance - Unipolar		15			15		kΩ
Compliance			±2.5			±2.5	Volts
INTERNAL REFERENCE VOLTAGE		+6.3			+6.3		Volts
Maximum External Current(8)			±200			±200	μA
Tempco of Drift, max		±10	±20		±10	±20	ppm/°C
POWER SUPPLY SENSITIVITY							
+15V Supply		±0.02			±0.02		% of FSR/% Vs
-15V and +5V Supplies		±0.002			±0.002		% of FSR/% Vs
POWER SUPPLY REQUIREMENTS							
DAC80	±14, +4.75	±15, +5	±16, +16	±14, +4.75	±15, +5	±16, +16	VDC
DAC80Z(7)	±11.4, +4.75	±12, +5	±16, +16	±11.4, +4.75	±12, +5	±16, +16	VDC
Supply Drain							
±15V/±12V (including 5mA load)		±25	±35		±25	±35	mA
+5V (logic supply)		+20	±30		+20	±30	mA
TEMPERATURE RANGE							
Specification	0		+70	0		+70	°C
Operating (double above specs)	-25		+85	-25		+85	°C
Storage	-55		+100	-55		+100	°C

NOTES:

1. Adding external CMOS hex buffers CD 4009A will provide CMOS input compatibility.
2. Adjustable to zero with external trim potentiometer.
3. FSR means "Full Scale Range" and is 20V for ±10V range, 10V for ±5V range, etc.
4. To maintain drift spec internal feedback resistors must be used for current output models.
5. See "Computing Total Accuracy Over Temperature."
6. With gain and offset errors adjusted to zero at 25°C. See discussion on last page.
7. DAC80Z supply range is ±12.0V min to ±16.0V max for 0 to +10V and ±10V outputs.
8. Maximum with no degradation of specifications.

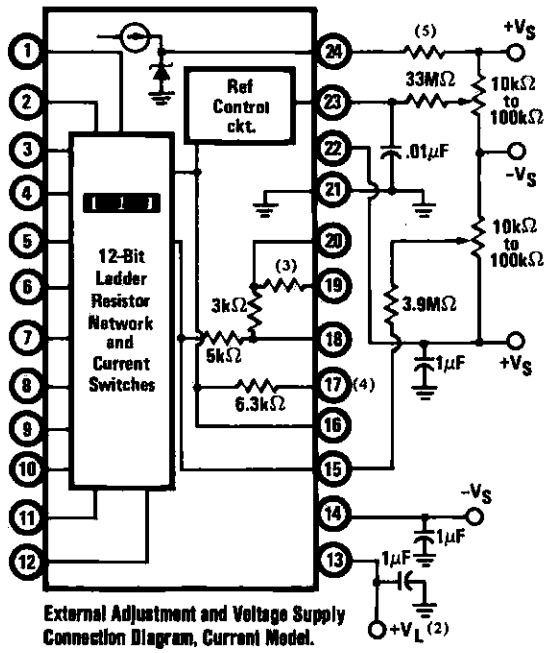
CONNECTION DIAGRAMS

VOLTAGE MODEL



External Adjustment and Voltage Supply Connection Diagram, Voltage Model.

CURRENT MODEL



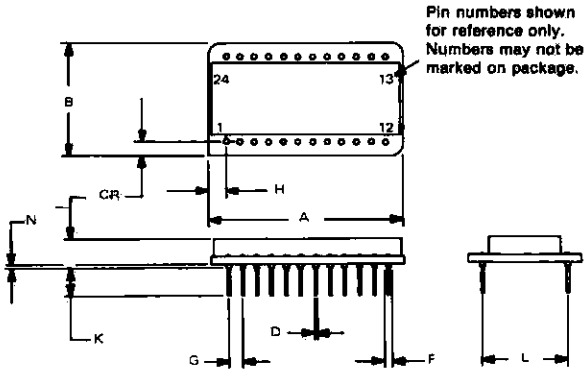
External Adjustment and Voltage Supply Connection Diagram, Current Model.

NOTES:
1. 3kΩ for CCD models, 5kΩ for CBI models.
2. If connected to+Vs,which is permissible,power dissipation increases 200mW.
3. CBI model, 2kΩ; CCD model, 0Ω and pin 20 has no internal connection.
4. 6.3kΩ resistor internally grounded on CCD models.
5. Resistor required only for Z models, see "Operating Instructions" Make no connection to power supply on non-Z models.

PIN ASSIGNMENTS

I Models	Pin No.	V Models
(MSB) Bit 1	1	Bit 1 (MSB)
Bit 2	2	Bit 2
Bit 3	3	Bit 3
Bit 4	4	Bit 4
Bit 5	5	Bit 5
Bit 6	6	Bit 6
Bit 7	7	Bit 7
Bit 8	8	Bit 8
Bit 9	9	Bit 9
Bit 10	10	Bit 10
Bit 11	11	Bit 11
(LSB) Bit 12	12	Bit 12 (LSB)
LOGIC SUPPLY	13	LOGIC SUPPLY
-Vs	14	-Vs
IOUT	15	VOUT
REF. INPUT	16	REF. INPUT
BIPOLAR OFFSET	17	BIPOLAR OFFSET
SCALING NETWORK	18	10V RANGE
SCALING NETWORK	19	20V RANGE
SCALING NETWORK	20	SUMMING JUNCTION
COMMON	21	COMMON
+Vs	22	+Vs
GAIN ADJUST	23	GAIN ADJUST
6.3V REF. OUT	24	6.3V REF. OUT

MECHANICAL



NOTE:
Leads ±1 true position within .010" (.25mm)R at MMC at seating plane.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.310	1.360	33.27	34.54
B	.770	.810	19.56	20.57
C	.150	.210	3.81	5.33
D	.018	.021	0.46	0.53
F	.035	.050	0.89	1.27
G	.100 BASIC		2.54 BASIC	
H	.110	.130	2.79	3.30
K	.150	.250	3.81	6.35
L	.600 BASIC		15.24 BASIC	
N	.002	.010	0.05	0.25
R	085	.105	2.16	2.67

CASE: Ceramic
MATING CONNECTOR: 245MC
PIN: Pin material and plating composition conform to method 2003 (solderability) of MIL-STD-883 (except paragraph 3.2).
WEIGHT: 8.4 grams (0.3 oz.)
HERMETICITY: Conforms to method 1014 condition C step 1 (fluorocarbon) of MIL-STD-883 (gross leak).

DISCUSSION

DIGITAL INPUT CODES

The DAC80 accepts complementary digital input codes in either binary (CBI) or decimal (CCD) format. The CBI model may be connected by the user for any one of three complementary codes: CSB, CTC or COB.

TABLE I. Digital Input Codes.

DIGITAL INPUT		ANALOG OUTOUT		
		CSB Compl. Straight Binary	COB Compl. Offset Binary	CTC* Compl. Two's Compl.
CBI Models	MSB LSB 000000000000 011111111111 100000000000 111111111111	+Full Scale +1/2 Full Scale Mid-scale -1LSB Zero	+Full Scale Zero -1LSB -Full Scale	-LSB -Full Scale -Full Scale Zero
CCD Models	MSB LSB	CCD Complementary Coded Decimal - 3 Digits		
	0110 0110 0110 1111 1111 1111	+Full Scale Zero		

* Invert the MSB of the COB code with an external inverter to obtain CTC code.

ACCURACY

Linearity of a D/A converter is the true measure of its performance. The linearity error of the DAC80 is specified over its entire temperature range. This means that the analog output will not vary by more than ±1/2LSB, maximum, from an ideal straight line drawn between the end points (inputs all "1"s and all "0"s) over the specified temperature range of 0°C to +70°C.

Differential linearity error of a D/A converter is the deviation from an ideal 1LSB voltage change from one adjacent output state to the next. A differential linearity error specification of ±1/2LSB means that the output voltage step sizes can range from 1/2LSB to 3/2LSB when the input changes from one adjacent input state to the next.

Monotonicity over a 0°C to +70°C range is guaranteed in the DAC80 to insure that the analog output will increase or remain the same for increasing input digital codes.

DRIFT

Gain Drift is a measure of the change in the full scale range output over temperature expressed in parts per million per °C (ppm/°C). Gain drift is established by: 1) testing the end point differences for each DAC80 model at 0°C, +25°C and +70°C; 2) calculating the gain error with respect to the 25°C value and; 3) dividing by the temperature change. This figure is expressed in ppm/°C and is given in the electrical specifications both with and without internal reference.

Offset Drift is a measure of the actual change in output with all "1"s on the input over the specified temperature range. The offset is measured at 0°C, +25°C and +70°C. The maximum change in Offset is referenced to the Offset at 25°C and is divided by the temperature range. This drift is expressed in parts per million of full scale range per °C (ppm of FSR/°C).

SETTLING TIME

Settling time for each DAC80 model is the total time (including slew time) required for the output to settle within an error band around its final value after a change in input (see Figure 1).

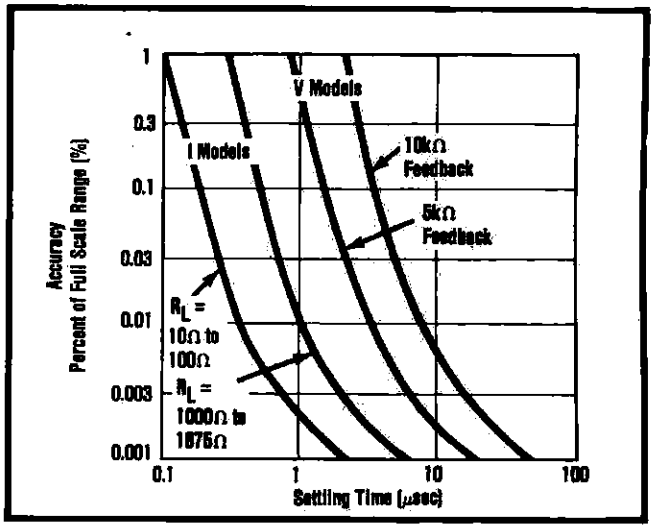


FIGURE 1. Full Scale Range Settling Time vs Accuracy.

Voltage Output Models: Three settling times are specified to ±0.01% of full scale range (FSR); two for maximum full scale range changes of 20V, 10V and one for a 1LSB change. The 1LSB change is measured at the major carry (0111...11 to 1000...00), the point at which the worst case settling time occurs.

Current Output Models: Two settling times are specified to ±0.01% of FSR. Each is given for current models connected with two different resistive loads: 10Ω to 100Ω and 1000Ω to 1875Ω. Internal resistors are provided for connecting nominal load resistances of approximately 1000Ω to 1800Ω for output voltage range of ±1V and 0 to -2V. See Table IV.

COMPLIANCE

Compliance voltage is the maximum voltage swing allowed on the current output node in order to maintain specified accuracy. The maximum compliance voltage of all current output models is ±2.5V. Maximum safe voltage swing permitted without damage to the DAC80 is ±5V.

POWER SUPPLY SENSITIVITY

Power supply sensitivity is a measure of the effect of a power supply change on the D/A converter output. It is defined as a percent of FSR per percent of change in

either the positive, negative, or logic supplies about the nominal power supply voltages (see Figure 2).

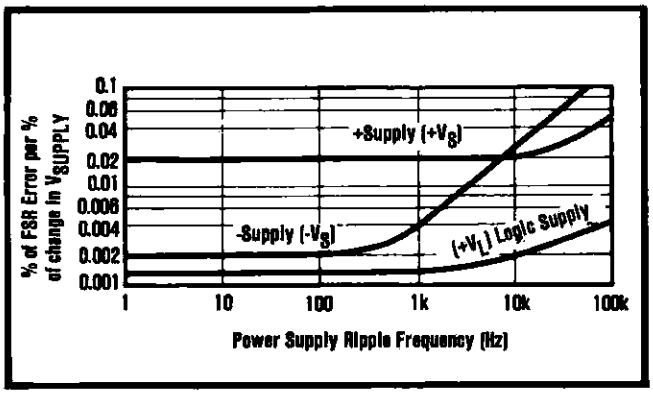


FIGURE 2. Power Supply Rejection vs Power Supply Ripple.

REFERENCE SUPPLY

All DAC80 models are supplied with an internal 6.3 volt reference voltage supply. This voltage (pin 24) has a tolerance of ±5% and must be connected to the Reference Input (pin 16) for specified operation. This reference may be used externally also, but external current drain is limited to 200μA. An external buffer amplifier is recommended if this reference will be used to drive other system components.

OPERATING INSTRUCTIONS

±12 VOLT SUPPLY OPERATION

The Z models will operate with supply voltages as low as ±11.4V. For operation with supplies less than ±14V an external resistor must be connected between the positive supply and pin 24. This provides additional current required by the internal reference. The required resistor value for supply voltages of ±11.4V to ±12.6V is 2.0kΩ and for supplies of ±12.6V to ±14V is 3.9kΩ.

It is recommended that output voltage ranges -10V to +10V and 0 to +10V not be used with the Z model if the supply voltages are ever less than the recommended ±12V. The output amplifier may saturate if $|V_{supply}| - |V_{out}\ max| < 2.0V$. This applies to units with both CBI and CCD input codes. Except for operation at lower supply voltages, the DAC80Z and DAC80 operation is identical.

POWER SUPPLY CONNECTIONS

Decoupling: For optimum performance and noise rejection, power supply decoupling capacitors should be added as shown in the Connection Diagrams. These capacitors (1μF tantalum or electrolytic recommended) should be located close to the DAC80. Electrolytic capacitors, if used, should be paralleled with 0.01μF ceramic capacitors for best high frequency performance.

EXTERNAL OFFSET AND GAIN ADJUSTMENT

Offset and gain may be trimmed by installing external Offset and Gain potentiometers. Connect these potentiometers as shown in the connection diagrams and adjust as described below. TCR of the potentiometers should be 100ppm/°C or less. The 3.9MΩ and 33MΩ resistors (20% carbon or better) should be located close to the DAC80 to prevent noise pickup. If it is not convenient to use these high value resistors, an equivalent "T" network, as shown in Figure 3, may be substituted in each case. The Gain Adjust (pin 23) is a high impedance point and a 0.001μF to 0.01μF ceramic capacitor should be connected from this pin to Common (pin 21) to prevent noise pickup. Refer to Figures 4 and 5 for relationship of Offset and Gain adjustments to unipolar and bipolar D/A converters.

Offset Adjustment: For unipolar (CSB, CCD) configurations, apply the digital input code that should produce zero potential output and adjust the Offset potentiometer for zero output.

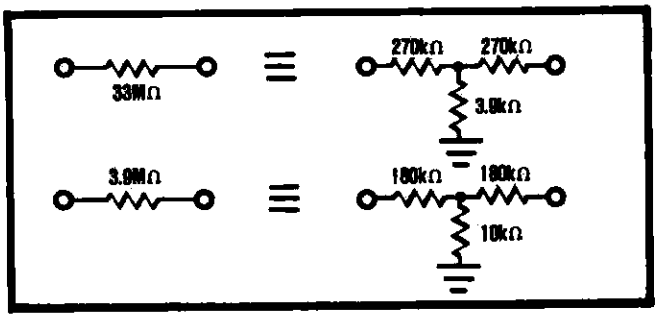


FIGURE 3. Equivalent Resistance.

For bipolar (COB, CTC) configurations, apply the digital input code that should produce the maximum negative output voltage. Example: If the Full Scale Range is connected for 20V, the maximum negative output voltage is -10V. See Table II for corresponding codes and the Connection Diagrams for offset adjustment connections.

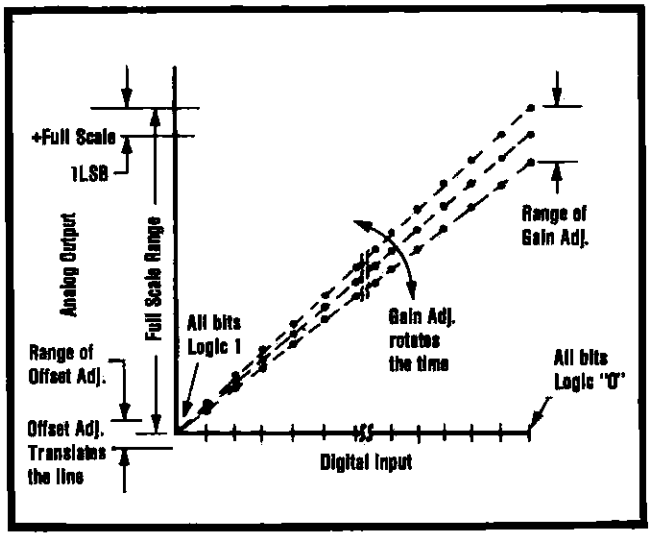


FIGURE 4. Relationship of Offset and Gain Adjustments for a Unipolar D/A Converter.

TABLE II. Digital Input/Analog Output.

	DIGITAL INPUT	ANALOG OUTPUT			
		VOLTAGE*		CURRENT	
		0 to +10V	±10V	0 to -2mA	±1mA
CBI Models	12-Bit Resolution MSB LSB				
	000000000000	+9.9976V	+9.9951V	-1.9995mA	-0.9995mA
	011111111111	+5.0000V	0.0000V	-1.0000mA	0.0000mA
	100000000000	+4.9976V	-0.0049V	-0.9995mA	+0.0005mA
	111111111111	0.0000V	-10.0000V	0.0000mA	+1.000mA
	One LSB	2.44mV	4.88mV	0.488μA	0.488μA
CCD Models	3-Digital Resolution MSB LSB				
	0110 0110 0110	+9.990V**	N/A	-1.249mA	N/A
	0110 0110 1111	+9.900V	N/A	-1.238mA	N/A
	0110 1111 1111	+9.000V	N/A	-1.125mA	N/A
	1111 1111 1111	0.000V	N/A	0.000mA	N/A
	One LSB	10.00mV	N/A	* 1.25μA	N/A

*To obtain values for other binary (CBI) ranges: 0 to +5V range: divide 0 to +10V range values by 2.
±5V range: divide ±10V range values by 2.
±2.5V range: divide ±10V range values by 4.

**Normal Full Scale Range with correct codes; output can go higher if illegal codes are applied.

Gain Adjustment: For either unipolar or bipolar configurations, apply the digital input that should give the maximum positive voltage output. Adjust the Gain potentiometer for this positive full scale voltage. See Table II for positive full scale voltages and the Connection Diagrams for gain adjustment connections.

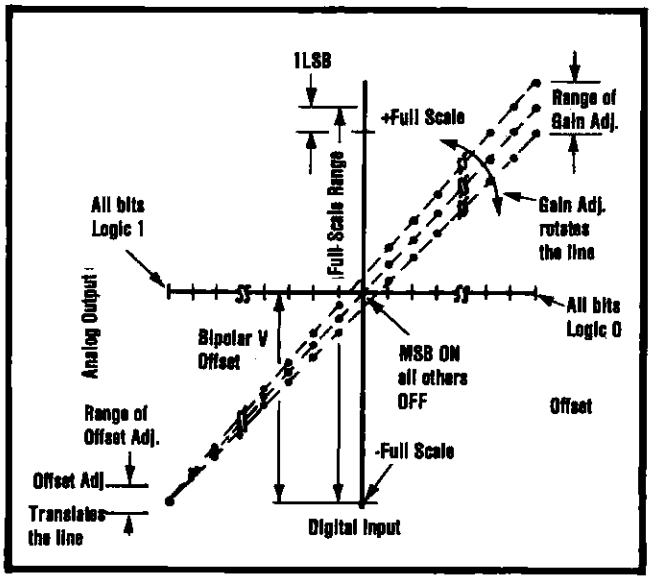


FIGURE 5. Relationship of Offset and Gain Adjustments for a Bipolar D/A Converter.

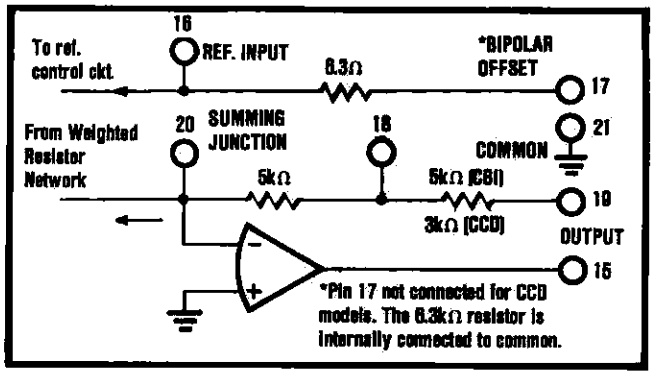


FIGURE 6. Output Amplifier Voltage Range Scaling Circuit.

VOLTAGE OUTPUT MODELS

OUTPUT RANGE CONNECTIONS

Internal scaling resistors provided in the DAC80 may be connected to produce bipolar output voltage ranges of ±10V*, ±5V or ±2.5V or unipolar output voltage ranges of 0 to +5V or 0 to +10V*. See Figure 6.

*Refer to ±12V Supply Operation discussion.

Gain and offset drift are minimized in the DAC80 because of the thermal tracking of the scaling resistors with other device components. Connections for various output voltage ranges are shown in Table III. Settling time is specified for a full scale range change: 5 microseconds for 8kΩ or 10kΩ feedback resistors; 3 microseconds for a 5kΩ feedback resistor.

TABLE III. Output Voltage Range Connections - Voltage Model DAC80.

Output Range	Digital Input Codes	Connect Pin 15 to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10	COB or CTC	19	20	15	24
±5	COB or CTC	18	20	N.C.	24
±2.5V	COB or CTC	18	20	20	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	20	24
0 to +10V	CCD	19	N.C.	15	24

CURRENT OUTPUT MODELS

The equivalent output circuit and resistive scaling network of the current model differ from the voltage model and are shown in Figures 7 and 8. Instructions for using the DAC80-XXX-I with a resistor or an external op amp follow. External R_{LS} or R_{LP} resistors are required to produce exactly 0 to -2V or ±1V output. TCR of these resistors should be ±100ppm/°C or less to maintain the DAC80 output specifications. If exact output ranges are not required, the external resistors are not needed.

Internal resistors are provided to scale an external op amp or to configure a resistive load to offer two output voltage ranges of ±1V or 0 to -2V. These resistors (R_{LI}) are an integral part of the DAC80 and maintain gain and bipolar offset drift specifications. If the internal resistors are not used, external R_L (or R_F) resistors should have a TCR of ±25 ppm/°C or less to minimize drift. This will typically add ±50 ppm/°C + the TCR of R_L (or R_F) to the total drift.

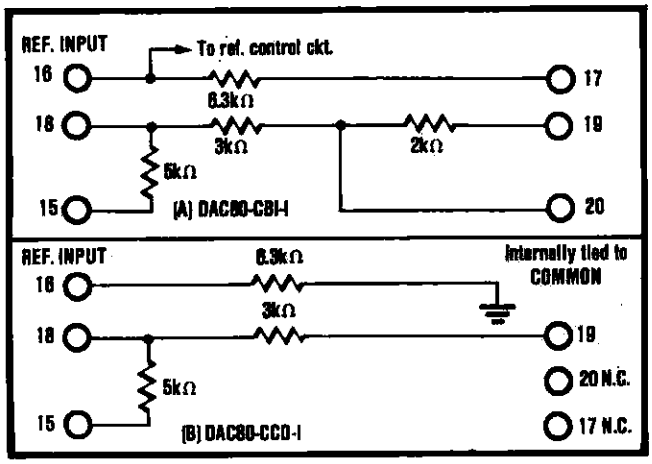


FIGURE 7. Internal Scaling Resistors.

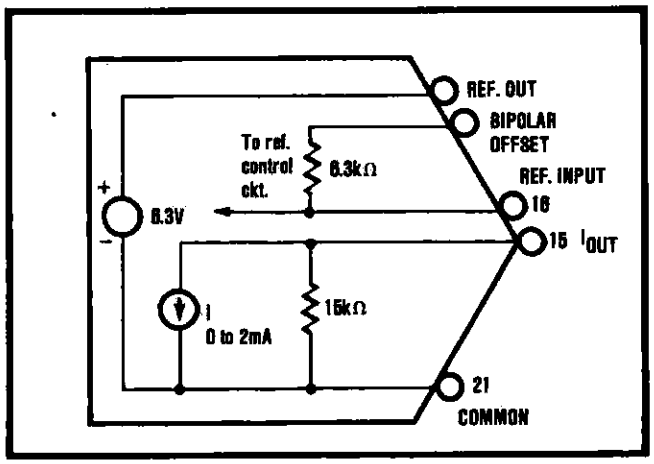


FIGURE 8. DAC80 Current Model Equivalent Output Circuit.

DRIVING A RESISTIVE LOAD UNIPOLAR

A load resistance, $R_L = R_{LI} + R_{LS}$, connected as shown in Figure 9 will generate a voltage range, V_{OUT}, determined by:

$$V_{OUT} = -2mA \left(\frac{15k\Omega \times R_L}{15k\Omega + R_L} \right)$$

Where R_L max = 1.36kΩ
and V_{OUT} max = -2.5V

To achieve specified drift, connect the internal scaling resistor (R_{LI}) as shown in Table IV to an external metal film trim resistor (R_{LS}) to provide full scale output voltage range of 0 to -2V. With $R_{LS} = 0$, V_{OUT} = -1.82V.

CCD Input Code: Connect the internal scaling resistors as shown in Table IV and add an external metal film

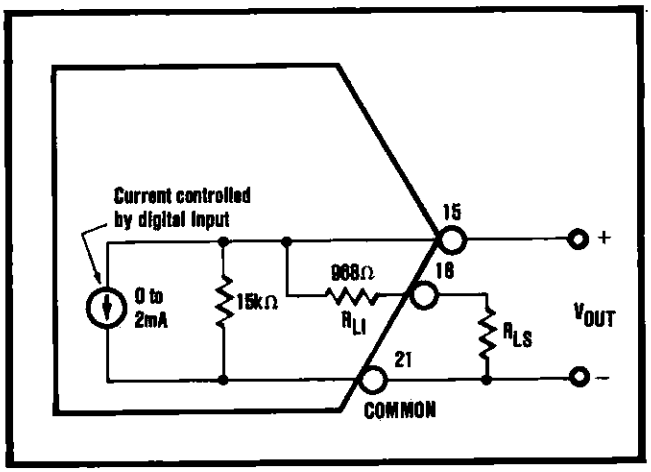


FIGURE 9. Equivalent Circuit DAC80-CBI-I Connected for Unipolar Voltage Output with Resistive Load.

TABLE IV. DAC80-XXX-I Resistive Load Connections.

Digital Input Codes	Output Range	Internal Resistance R_{LI}	1% Metal Film External Resistance R_{LS}	1% Metal Film External Resistance R_{LP}	R_{LI} Connections: Connect Pin 15 to	R_{LI} Connections: Connect Pin 18 to	R_{LI} Connections: Connect Pin 20 to	Reference: Connect Pin 16 to	Bipolar Offset: Connect Pin 17 to	Bipolar Offset: R_{LS}	Bipolar Offset: R_{LP}
CSB	0 to -2V	0.968kΩ	105Ω	N/A	20	19 & R_{LS}	15	24	Com (21)	Between Pin 18 & Com (21)	N/A
CCD	0 to -2V	1.875kΩ	N/A	36.5kΩ	19	Com (21)	N.C.	24	N.C	N/A	Between Pin 15 & 21
COB or CTC	±1V	1.2kΩ	90.9Ω	N/A	18	19	R_{LS}	24	15	Between Pin 20 & Com (21)	N/A

resistor (R_{LP}) in parallel as shown in Figure 10 to obtain a 0 to -2V full scale output voltage range for CCD input codes:

$$\text{With } R_L = \frac{R_{LI} \times R_{LP}}{R_{LI} + R_{LP}}$$

$$V_{OUT} = -1.25\text{mA} \left(\frac{15.6\text{k}\Omega \times R_L}{15.6\text{k}\Omega + R_L} \right)$$

If $R_{LP} = \infty$, $V_{OUT} = -2.08\text{V}$

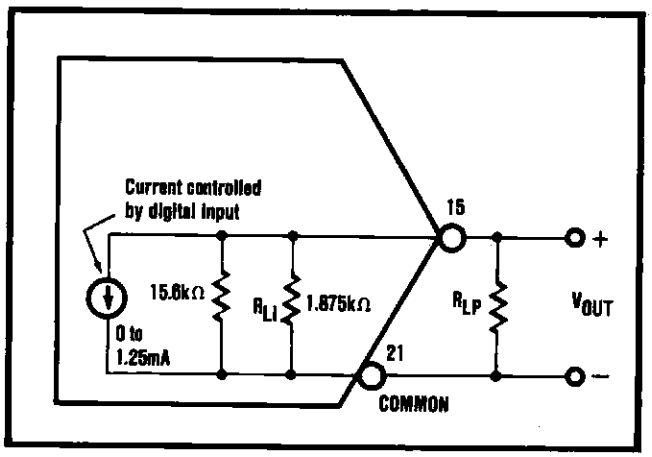


FIGURE 10. DAC80-CCD-I Connected for Voltage Output with Resistive Load.

DRIVING A RESISTOR LOAD BIPOLAR

The equivalent ouptut circuit for a bipolar output voltage range is shown in Figure 11, $R_L = R_{LI} + R_{LS}$. V_{OUT} is determined by:

$$V_{OUT} = \pm 1\text{mA} \left(\frac{R_L \times 4.44\text{k}\Omega}{R_L + 4.44\text{k}\Omega} \right)$$

Where R_L max = 5.72kΩ

V_{OUT} max = ±2.5V

To achieve specified drift, connect the internal scaling resistors (R_{LI}) as shown in Table IV for the COB or CTC

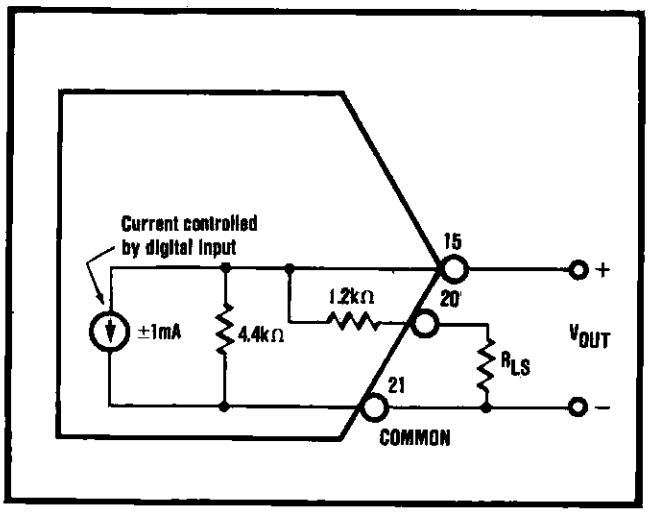


FIGURE 11. DAC80-CBI-I Connected for Bipolar Output Voltage with Resistive Load.

codes and add an external metal film resistor (R_{LS}) in series to obtain a full scale output range of ±1V.

With $R_{LS} = 0$, $V_{OUT} = \pm 0.944\text{V}$.

DRIVING AN EXTERNAL OP AMP

The current model DAC80 will drive the summing junction of an op amp used as a current to voltage converter to produce an output voltage. See Figure 12.

$$V_{OUT} = I_{OUT} \times R_F$$

where I_{OUT} is the DAC80 output current and R_F is the feedback resistor. Using the internal feedback resistors of the current model DAC80 provides output voltage ranges the same as the voltage model DAC80. To obtain the desired output voltage range when connecting an external op amp, refer to Table V.

TABLE V. Voltage Range of Current Output DAC80.

Output Range	Digital Input Codes	Connect Ⓐ to	Connect Pin 17 to	Connect Pin 19 to	Connect Pin 16 to
±10V	COB or CTC	19	15	Ⓐ	24
±5V	COB or CTC	18	15	N.C.	24
±2.5V	COB or CTC	18	15	15	24
0 to +10V	CSB	18	21	N.C.	24
0 to +5V	CSB	18	21	15	24
0 to +10V	CCD	19	N.C.	Ⓐ	24

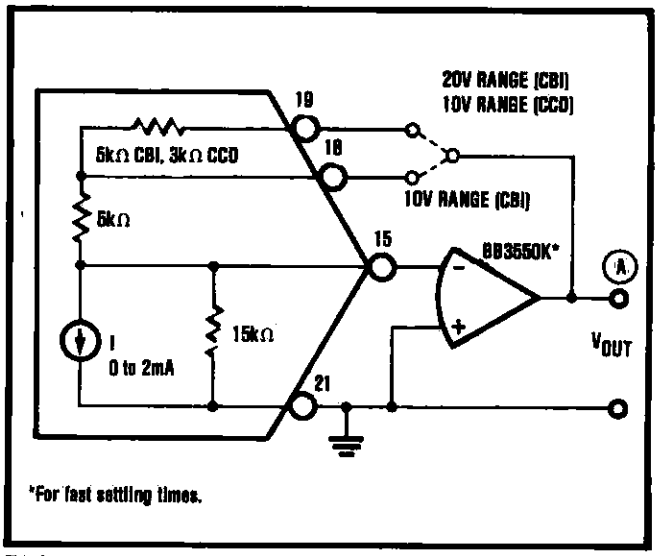


FIGURE 12. External Op Amp - Using Internal Feedback Resistors.

OUTPUT LARGER THAN 20V RANGE

For output voltage ranges larger than ±10V, a high voltage op amp may be employed with an external feedback resistor. Use I_{OUT} values of ±1mA for bipolar voltage ranges and -2mA for unipolar voltage ranges. See Figure 13. Use protection diodes when a high voltage op amp is used.

The feedback resistor, R_F, should have a temperature coefficient as low as possible. Using an external feedback resistor, overall drift of the circuit increases due to the

lack of temperature tracking between R_F and the internal scaling resistor network. This will typically add 50 ppm/°C + R_F drift to total drift.

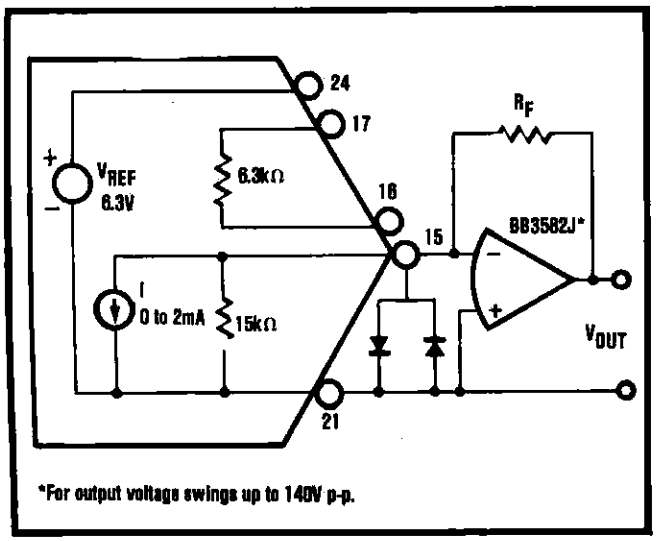


FIGURE 13. External Op Amp - Using External Feedback Resistors.

COMPUTING TOTAL ACCURACY OVER TEMPERATURE

The accuracy drift with temperature of a DAC80 consists of three primary components: Gain drift, unipolar or bipolar offset drift, and linearity drift. To obtain the worst case accuracy drift, most users would assume that all drift errors are random and would simply add them algebraically. However, the worst case accuracy drift for a DAC80 operating in the bipolar mode is about one-half of the algebraic sum of the individual drift errors.

To explain this fact, it is necessary to consider the unipolar and bipolar modes of operation separately. Note that the linearity drift of both modes is negligible. (Total linearity error is less than ±1/2LSB over 0°C to +70°C.)

In the unipolar mode of operation, offset drift (±1 ppm/°C) is due primarily to voltage offset drift of the output op amp and, to a lesser extent, to the leakage current through the quad current switches. Gain drift consists of several components: 1) ±10 ppm/°C due to ratio drift of current weighting resistors to the reference resistor and current switch V_{BE} to the reference transistor (refer to Model 4550 data sheet); and 2) ±20 ppm/°C due to the zener reference. The sum of these two components, ±30 ppm/°C, is the maximum gain drift.

Because the parameters described could all drift in the same direction, the worst case accuracy drift in the unipolar mode is simply the sum of the components, or ±31 ppm/°C.

In the bipolar mode the major portion (67%) of gain drift is due to the zener reference. The gain and offset drifts caused by reference drift are always in opposite directions. Therefore, the accuracy drift will be the difference rather than the sum of these drifts.

First, consider the effect of reference variations on offset drift. Figure 14 shows a simplified circuit diagram of a DAC80 operating in the bipolar mode with all bits off. The current switch leakage current is negligible, so

$$V_{\text{-FULL SCALE}} = -\frac{R_F}{R_{BPO}} \times V_{REF}$$

$$= -\frac{10k\Omega}{6.3k\Omega} \bullet 6.3V = -10V$$

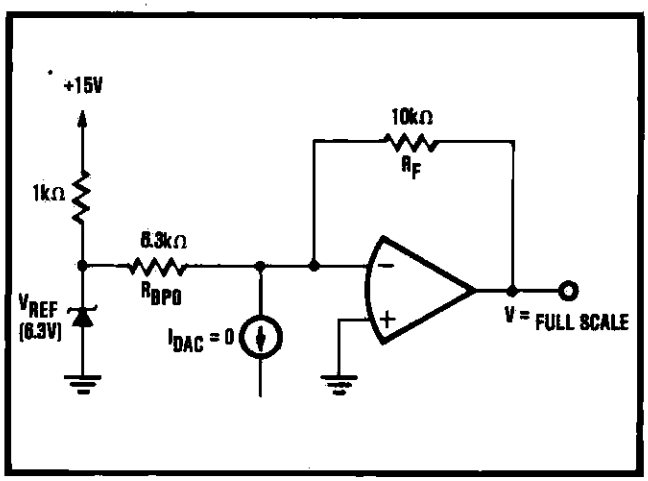


FIGURE 14. Simplified Diagram of DAC80 with "All Bits Off" Operating in Bipolar ±10V Range.

This equation shows that if V_{REF} increases, the output voltage will decrease and vice versa. If the V_{REF} drift is +20 ppm/°C, this is equivalent to (+20 ppm/°C) x (+6.3V) = +126μV/°C. This will result in a voltage drift at the amplifier output of

$$\frac{\Delta V_{-FS}}{\Delta T} = -\frac{R_F}{R_{BPO}} \bullet \frac{\Delta V_{REF}}{\Delta T}$$

$$= -\frac{10k\Omega}{6.3k\Omega} \bullet 126\mu V/°C = -200\mu V/°C.$$

Since the DAC80 is operating in the ±10V range this is equivalent to (-200μV/°C) ÷ (20V range) = -10 ppm of FSR/°C.

Now consider the effect of reference changes on gain drift. When all the bits are turned on it can be shown that:

$$\frac{\Delta V_{+\text{FULL SCALE}}}{\Delta T} = +\frac{R_F}{R_{BPO}} \bullet \frac{V_{REF}}{\Delta T}$$

$$= +\frac{10k\Omega}{6.3k\Omega} \bullet 126\mu V/°C = +200\mu V/°C$$

$$\text{and } \frac{+200\mu V/°C}{20V \text{ Range}} = +10\text{ppm/°C of FSR.}$$

This result indicates that the drift of the minus full scale voltage will be equal in magnitude to, and in the opposite direction of, the drift of the plus full scale voltage and that zener reference variations have virtually no effect on the zero point (see Figure 15). This equation also indicates that the gain drift is equal to the V_{REF} drift in ppm/°C, and the magnitude of the minus full scale drift and plus full scale drift is equal to one-half of the V_{REF} drift.

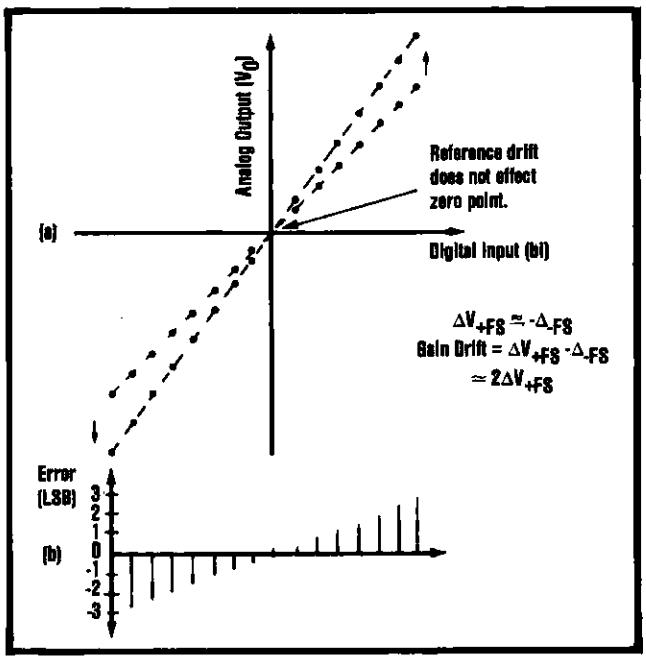


FIGURE 15. (a) Effect of a Positive Reference Drift on the Ideal D/A Transfer Function; (b) Error Distribution Due to Reference Voltage Drift in a DAC80.

Using this relationship, the worst case accuracy drift for a bipolar DAC80 can be computed. The maximum TCR of the zener reference is ±20ppm/°C. The gain drift due to the reference then is also ±20ppm/°C. The full scale drift and bipolar offset drift are each half that amount or ±10ppm/°C. The maximum gain and offset drifts of the DAC80, exclusive of the reference, are ±10ppm/°C and ±5ppm/°C respectively. Adding this to the full scale drift due to the reference gives a worst case total accuracy drift of ±25ppm/°C. (Random drifts, which these are, can be in the same direction, so they add directly.) This is much less than the total drift obtained by simply adding the maximum gain and bipolar offset drifts (±45ppm/°C). The maximum zero point drift is equal to one-half of the gain drift exclusive of the reference plus the offset drift exclusive of the reference, or ±10ppm of FSR/°C.

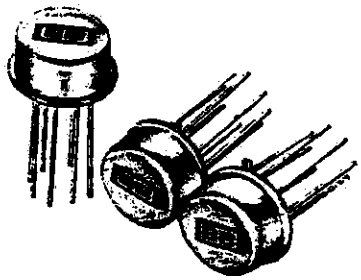
The DAC80 is specified over a 0°C to +70°C temperature range giving a maximum excursion from room temperature (+25°C) of 45°C. Assuming that gain and offset errors have been adjusted to zero at room temperature,

total worst case accuracy error
= Linearity error + Accuracy drift x ΔT
= ±0.01% + ±25ppm/°C (45°C)(100)
= ±0.12%;

total worst case bipolar zero point error
= Bipolar zero drift x ΔT
= ±10ppm of FSR% (45°C)(100)
= ±0.045%.

ORDERING INFORMATION

DAC80	X	–	XXX	–	X
Low Cost 12-Bit D/A Converter Family Example: DAC80-CBI-V Binary DAC80 with voltage output	Z = Wide Supply Range Blank = Standard		INPUT CODE CBI = Complementary 12-bit binary CCD = Complementary 3-digit BCD		OUTPUT V = Voltage I = Current



SHC298AM

LOW COST MONOLITHIC SAMPLE-HOLD AMPLIFIER

- 12 Bit Throughput Accuracy
- Less Than 10 μsec Acquisition Time
- Wideband Noise Less Than 20 μV rms
- Reliable Monolithic Construction
- $10^{10}\,\Omega$ Input Resistance
- TTL/PMOS/CMOS Compatible Logic Input

DESCRIPTION

The SHC298AM is a high performance monolithic sample/hold circuit which features very high DC accuracy with fast acquisition times and a low droop rate. With the addition of one external holding capacitor, 12 bit accuracy can be achieved with a 6 microsecond acquisition time. Droop rates less than 5 millivolts per minute can be achieved with a one microfarad holding capacitor.

The fully differential logic inputs have low input currents, and are compatible with TTL, PMOS, and CMOS logic families. The input offset adjustment can be made using a single external potentiometer and resistor, and the adjustment does not degrade input offset drift.

The SHC298AM will operate with power supplies ranging from ±5 volts to ±18 volts. It is available in a hermetically sealed 8 lead low profile package, and is specified for a temperature range from -25 to +85°C. The SHC298AM is the best price/performance bargain in its class. It is well suited for use in data acquisition systems, data distribution systems, analog delay circuits, and pulse amplitude modulation circuits.

BURR-BROWN
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International Airport Industrial Park • P.O. Box 11400 • Tucson, Arizona 85734
Tel: 602-294-1431 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 66-6491

SPECIFICATIONS

Specifications at T_A = +25°C with rated supplies with 1000 pF holding capacitor unless otherwise noted.

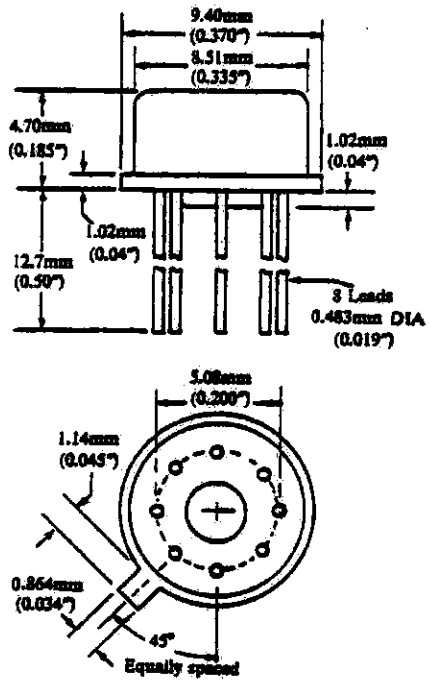
ELECTRICAL

MODELS	SHC298AM MIN	SHC298AM TYP	SHC298AM MAX	UNITS
INPUT				
ANALOG INPUT				
Voltage Range	±(V_{cc}-2.5)			Volts
Maximum Safe Input Signal		±V_{cc}		Volts
Resistance		10^{10}		Ohms
Bias Current		10	50	nA
DIGITAL INPUT				
Mode Control Truth Table	Pin 7 / Pin 8 / Circuit State			
	0V / +2.4V / Sample (Track)			
	0V / +0.8V / Hold			
	+2.4V / +2.8V / Hold			
	+0.8V / +2.8V / Sample (Track)			
Mode Control and Mode Control Reference Input Current			10	µA
Differential Logic Threshold		1.4		Volts
TRANSFER CHARACTERISTICS				
ACCURACY (25°)				
Throughput Nonlinearity for Hold Time < 1ms		±0.010	±0.015	% of 20V
Gain		+1.0		V/V
Gain Error		±0.004	±0.010	%
Input Voltage Offset (adj to zero)		±2	±7	mV
Droop Rate		±25	±125	µV/ms
Charge Offset		±15	±25	mV
Noise (rms) 10 Hz to 100 kHz		10	20	µV
Power Supply Rejection		±25	±50	µV/V
ACCURACY DRIFT				
Gain Drift		3	4	ppm/°C
Input Offset Drift		15	45	µV/°C
Charge Offset Drift C = 1000 pF		50	150	µV/°C
C = 10,000 pF		20	50	µV/°C
Droop Rate at T_A = +85°C		1	10	mV/ms
DYNAMIC CHARACTERISTICS				
Full Power Bandwidth, C = 1000 pF	75	125		kHz
C = 10,000 pF	10	16		kHz
Output Slew Rate, C = 1000 pF	7	10		V/µs
C = 10,000 pF	1.4	2		V/µs
Aperture Time				
Negative Input Step		125	200	ns
Positive Input Step		30	45	ns
Acquisition Time (C = 1000 pF)				
to ±0.01%, 10V step		6	10	µs
to ±0.01%, 20V step		8	12	µs
to ± 0.1%, 10V step		5	9	µs
to ±0.1%, 20V step		7	11	µs
Sample-to-Hold Transient				
Peak Amplitude		160		mV
Settling to 1 mV		1.0	1.5	µs
Feedthrough (Response to 10V Input Step)		±0.007	±0.015	% of 20V
OUTPUT				
ANALOG OUTPUT				
Voltage Range	±(V_{cc}-2.5)			Volts
Current Range	±2			mA
Impedance		0.5	4	Ohms
TEMPERATURE				
Specification		-25 to +85		°C
Operating		-55 to +125		°C
Storage		-55 to +150		°C
POWER SUPPLY				
Rated Voltage		±15		VDC
Range[1]	±4.75		±18	VDC
Current		±4.5	±6.5	mA
PRICES 1 - 24		$7.95		
25 - 99		$6.90		

Prices and specifications subject to change without notice.

(1) Logic voltage on pin 8 should not exceed V_{cc} - 1 volt.

MECHANICAL

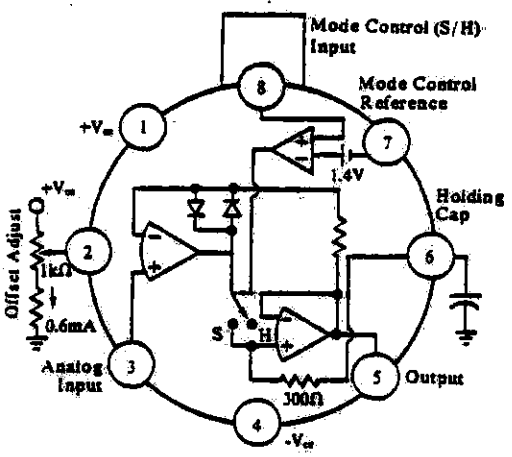


Pin Material and Plating Composition: Conforms to Mil-Std-883 Method 2003 (solderability)

Hermeticity: Conforms to Mil-Std-883, method 1014, Condition C, Step 1. Fluorocarbon (gross leak) and method 1014, Condition A, Helium, 5 x 10^{-8} cc/sec (fine leak)

Connector: None

PIN CONFIGURATION



(TOP VIEW)