OHIO SCIENTIFIC

Manual for

Model 500 CPU

Part 1

INTRODUCTION TO SMALL COMPUTER HARDWARE

Small computers are made up of several modules, or blocks. The first of these, the microprocessor, is an integrated circuit much like those used in modern watches and calculators. It performs the function of a large computer, which a few years ago would have been prohibitively expensive. This integrated circuit makes the whole field of personal computing possible and affordable.

Next, one must have some memory, which can be in the form of ROM, PROM, EPROM, or RAM. The first three devices provide permanent storage of programs and data, that is, they do not "forget" when the power is turned off. RAM provides modifiable storage, that is, programs and data can be written in and read out repeatedly. However, almost all types of RAM "forget" whenever the power is turned off. Therefore, RAM is used for temporary storage, and ROM, PROM, and EPROM are used for permanent storage of programs which will not change. Generally, a small computer will have a large amount of RAM for general purposes, and very little PROM or ROM. It does need some of the latter, to give it some intelligence when it is first turned on, and this is usually in the form of a monitor program which allows the user to load additional programs from some external device such as a tape recorder into RAM. Today, the most advanced computers put BASIC, the most commonly used programming language in ROM. This has only recently become possible because BASIC requires approximately 8,000 bytes of ROM, which had been a costly feature until now.

Along with memory, the microprocessor requires some form of I/O device (Input/Output), that is, some way of "talking" to the outside world. The computer communicates through interfaces such as the ACIA-Based Serial Interface and the PIA-Based Parallel Interface to external devices called peripherals, such as CRT terminals, Teletypes, paper tape readers, paper tape punches, line printers, and audio cassettes. Other types of interfaces include D/A converters and A/D converters.

The microprocessor communicates with its interfaces and memory with a series of wires, or lines, called buses. There are generally three buses in any microcomputer: an address bus, a data bus, and a control bus. These three buses are combined in what is called a system bus.

The address bus is generally made up of 16 lines. The microprocessor always is the signal generator for this bus. The 16 lines carry specific addresses, that is, 16-bit binary words which select a memory or I/O location. This location can be thought of as a post office box, and the address word can be thought of as the box number. The microprocessor can, therefore, through its address bus, specify memory or I/O locations.

It can place data in these locations, or read memory from them via an 8-bit wide data bus. Its 8-bit width indicates that the microcomputer can read or write one byte at a time. With ROMs, PROMs, and EPROMs, the microcomputer only reads what is already in those locations, and acts accordingly. In the case of RAM and some I/O locations, the microprocessor can also place data in these locations. Unless the computer has a large amount of ROM, it will generally be very "stupid" when first turned on. That is, its main memory, or RAM, has nothing of value in it. The user must enter a program which the microcomputer can then execute in its RAM memory. It does this by use of a PROM Monitor Program, that is, a short program which the computer runs, allowing it to take data from some interface, and ultimately from some peripheral, and place it into its operating memory, or RAM. It can then later perform functions and write or store additional programs based on this stored program. The typical peripherals used for this are a video display interface, and a keyboard, or a Teletype or CRT terminal. Additional mass storage devices, such as paper tape readers, audio cassettes, and floppy disks, are utilized for storage of programs.

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The OSI system utilizes a 48-line system bus made up of an address bus of from 16 to 20 lines (depending on the CPU board used in the system), an 8-line data bus, a 7-line control bus, power connections, and spare lines for user connections. The system utilizes 8" x 10" PC boards plugged into an 8-slot backplane, which spaces the system boards one inch apart. For very small computers, the Model 500 can be used without a backplane board as a stand-alone computer, that is, it can be populated with the microprocessor, PROM and ROM memory, RAM memory, and a serial interface, so that it can function as a complete computer by itself. For larger systems, however, a backplane board and additional system boards are used.

It is necessary for anyone servicing or building an OSI system to be somewhat familiar with the 48-line bus utilized by the computer. This bus is outlined on page B-3

Glossary of Small Computer Terms

ACIA- (Asynchronous Communications Interface Adapter) An IC used for serial data transfer between a device such as a small computer and a serial terminal.

A/D- (Analog/Digital) refers to changing an analog signal to a digital signal which the computer can use.

Backplane Board- (Sometimes called mother board) allows simple interconnection between small computer boards using the same bus.

Bit- The smallest amount of data possible; a bit is expressed as a high or low (on or off) state (normally 1 or 0).

Bus- Refers to the set of foils or wires needed to interconnect between system boards provided that the pattern of how each of the connections is used is consistent for all system boards.

Byte- 8 bits of data. The most fundamental microprocessor commands are organized into sets of 8 bits (i.e. bytes).

CPU- (Central Processing Unit) the portion of a microprocessor which does the actual arithmetic calculations and decision making.

D/A- (Digital/Analog) Refers to changing digital signals (from the computer) into analog signals.

EPROM- (Erasable Programmable Read Only Memory) information stored in an EPROM IC can only be removed by special light sources or specific voltages (depending on the type of EPROM). Through the use of a special programming device, the user can store a set of information in the EPROM after it has been erased.

Hardware- that part of a computer consisting of actual electronic circuitry, printed circuit boards, case, and power supply as opposed to software which is the set of commands the hardware is executing.

I/O- (Input/Output) refers to bringing information into the machine in a form it recognizes and allowing the machine to transmit information. In other words, communicating with the outside world.

Memory- a general term referring to parts of the computer where information is stored.

Microprocessor- a large IC (electronic part) which functions as the CPU of the microcomputer. The 6502 on Ohio Scientific's 500 board is a microprocessor.

PC Board- (Printed Circuit Board) a card with foils (electronically conductive pathways) connecting electronic components which are mounted on the board.

PIA- (Peripheral Interface Adapter) IC used for parallel data transfer.

PROM- (Programmable Read Only Memory) Memory which can have information stored on it once, but, is not normally changeable.

RAM- (Random Access Memory) the data stored in this type of memory is easily changed by the user while the machine is in use (unlike ROM, PROM, EPROM) However, it is erased whenever electrical power is turned off.

ROM- (Read Only Memory) preprogrammed, unchangeable memory.

Software- programs or instructions that the machine will execute.

48 LINE SYSTEM BUS OUTLINE

B1 - low true WAIT When pulled low by a system board, causes processor clock to slow down to speed of approximately 500KHz on most processor boards. This is used to service slow memory and I/O devices.

B2 - NMI (non-maskable interrupt) When brought low, a non-blockable interrupt occurs, causing the processor to stop its operation and service this interrupt, that is, go to a specific memory location and start executing an interrupt service routine.

B3 - IRQ (interrupt request) An interrupt which can be masked by the processor, that is, the processor can choose to ignore this interrupt under program control. If the interrupt is not masked, it will cause the processor to stop executing the program it is in, and jump to a different location.

B4 - DD (data direction) When pulled low by system board, it changes the direction of the 8T26 buffers on the CPU board, and thus switches the processor from outputing data to the bus to listening to the bus.

B5 - D0
B6 - D1
B7 - D2
B8 - D3
B9 - D4
B10 - D5
B11 - D6
B12 - D7

Bi-directional eight-bit wide data bus for communication of data between the processor and system boards.

B13
B14
B15
B16

Upper data bits on some systems

B17 Optional reset line used to clear all PIAs and similar I/O circuitry in the system.

B18 spare line

B19
B20
B21
B22

Memory management address lines: Lines 21 and 22 are used on systems with a 500 CPU Board; all 4 are used with the 510.

B23 +12 Power connection

B24 -9 Power connection

B25
B26

+5 Power connection

B27
B28

Ground Connection

B29 - A6
B30 - A7
B31 - A5
B32 - A8
B33 - A9
B34 - A1
B35 - A2
B36 - A3
B37 - A4
B38 - A0

Ten low-order address lines

B39 - Ø2 Used to clock external circuits or external I/O interfaces, such as the A/D converter.

B40 - R/W (read/write) Originates at the microprocessor and specifies read or write operations on the data bus.

B41 - VMA (valid memory address) Only used in conjunction with the 6800 microcomputers. The 6502s always have this line high.
B42 - Ø2•VMA Master timing signal for enabling memory and I/O in the system.
B43 - A10
B44 - A11
B45 - A12
B46 - A13
B47 - A14
B48 - A15
} Six high-order address lines

Ohio Scientific offers a full family of boards which conform to its 48-line system bus. These boards are as follows:

500 CPU Board 6502 microprocessor, provisions for 8K ROM, 4K RAM, serial interface, optional parallel interface. Operates as stand-alone computer equivalent to 12K system, or as a CPU Board in a larger system.

510 CPU Board 6502, Z-80, 6800 microprocessors, including serial and parallel ports, and PROM Monitors. Designed for use with disk and external RAM.

RAM Boards
1) 420 (4K x 8 or 4K x 12) 2102-type
2) 520 (16K)
One RAM board is being developed with 65K dynamic memory.

EPROM Boards
1) 450 with 8K of 512-word EPROMs, with on-board programmer
2) 455 with 4K of 1702 devices.

I/O Boards
1) 430 with audio cassette interface, two D/A converters and A/D converters; can be selectively populated just for audio cassette.
2) 440 video graphics, providing inexpensive video display interface and keyboard port which can be optionally populated for graphics.
3) 470 floppy disk controller board
4) line-printer interface (Centronixs compatible)
5) multiple-port serial interface board.

Ohio Scientific also offers building blocks for multiprocessing, such as our highly advanced 560Z multiprocessor board, which allows multiple CPUs to be connected together, operating simultaneously. This CPU board must work in conjunction with a 6502-based CPU and has a Z-80 and/or a ~~6800~~ 6100 microprocessor on it. It can also be selectively populated as a porthole to connect two or more standard OSI systems together. Consult our most recent catalogs for details on OSI accessory boards and OSI peripherals and software.

Introduction:

The 500 represents the state of the art in single-board computers. It is fully compatible with all 400 series boards and the OSI 48-line bus, thus no older products now become obsolete. The Model 500 can accept eight 2K x 8 2616-type mask ROMS which contain our super-fast 8K BASIC by Microsoft. The Model 500 also has provisions for 4K of 2102-type memories, an ACIA-based serial interface which can be populated for RS-232 or 20 m.a. current loop at five different baud rates which are also jumper selectable.

The 500 can optionally have a PIA-based 16-line parallel I/O port, part of which is used for a 256K memory management unit controlling two additional address lines on the bus (A16 and A17). The 500 can also accept up to three 1702-type PROMS and can be populated for one, two, or three of these PROMS by partially or fully decoding the address base at FD, FE, and FFXX. The model also has full bus pullup resistors on board. The 500 can be used with our existing 65A, 65V, and floppy disk bootstrap PROMS. It is effective as a stand-alone computer which uses 8K BASIC with 4K of workspace, and is thus functionally equivalent to a 12K computer. It is offered fully assembled and tested, minus the PIA port, for $298 including the BASIC and ROM.

The board has many subtle points that will make it even more useful than is apparent so far. For example, there are provisions on the board for additional data direction and wait state diodes and address decoding so that the 500 board may be used as an accessory board in OSI computers. That is, the 4K of RAM memory can be addressed for some location other than location 0, and other ports can be placed at other addresses, so that the 500 board can be used as a combination ROM, RAM, EPROM, PIA, and ACIA board, along with another 500 or other board that has a processor on it. This allows for extremely high system density. The four sockets used for the 2616 mask ROM are programmable in function by two 16-bit dip locations, which are normally set up for 8K BASIC. By changing jumpers in these DIP locations, these four sockets can by changed to accept up to thirty different devices including the popular 2704, 2708, and 2716 UV erasable EPROMS. Thus, the board can be populated with 2K, 4K or 8K of user-programmed EPROM, instead of for BASIC. This in conjunction with the PIA makes this board extremely useful for dedicated industrial control applications.

Other features of the board include 256K addressing, or two additional address bit pager. This feature, along with an Expanded Monitor PROM Set which will soon be available, will allow up to four independent users in a 500-based system by flipping upper memory lines. The user programs can be switched in and out, thus allowing ultra-fast interrupt service and memory partitioning of users. The 8K BASIC ROMs also include a complete CRT routine and audio cassette drivers, so that by changing to a different support PROM the board can support BASIC in conjunction with a 440 Video Board. The system can support a 430B Based Cassette I/O board in either serial or video modes. Extra control characters in BASIC allow storage and retrieval of BASIC programs, even when the serial baud rate is lower than the cassette baud rate, by invoking printing or non-printing operations.

The 500 Board can be selectively populated to emulate any 400 Board, and is completely compatible with systems using the 400 Board.

500 Boards and Challenger IIs can also be used with disk drives, of course. However, the 8K BASIC in ROM is not suitable for use with disk as it does not have the disk I/O commands. Furthermore, BASIC can be quickly pulled in fromdisk instead of ROMs when the disk drive is present. We offer Challenger IIs without the BASIC ROMs and with the floppy disk instead.

The Model 500 can be broken down into several modules as shown in block diagram 1, System Overview. The 500 board must at least contain a 6502 microprocessor, a system clock to support it, address and data buffers, and a system monitor PROM, which will require support circuitry to be properly addressed. All other circuitry could be external to the 500 board on other OSI systems boards; furthermore, any combination of additional circuitry, or all of it, can be placed on the 500 board. It is particularly economical to place all the computer circuitry on a single board in a small system because this minimizes buffering and eliminates the expense of interconnections. The board can also have 4K RAM which requires buffers and additional enable circuitry for support. It can have 8K ROM or PROM with additional support circuitry and a conventional serial interface for standard computer terminals such as CRT terminals and Teletypes, and an optional 16-line parallel I/O port supported by a PIA. These circuits also require decoders.

Each of the blocks in the diagram has a number referring to the schematic of interest. The following is a detailed discussion of the actual circuitry.

Microprocessor, Clock, Address and Data Bus (diagram 2)

The 6502 Clock is provided by a dual one-shot operating as a multivibrator. The clock circuitry can be partially populated as a single-speed clock or fully populated as an adjustable two-speed clock. The only requirements for single-speed operations are the one-shot (IC-B2), the pullup resistor on its clear lines (R17), and the R10-C2 and R18-C3 R-C circuits.

For high performance operations, it will be necessary to have a low-speed mode on the clock for slow components in the system. This lower speed is actuated by the WAIT line, present on the system bus connector as B1. This additional circuitry is R11, R12, and adjustable potentiometer R50, the 7417 Buffer on IC-C2, and diodes D1 and D2. The clock can then be adjusted for high-speed operation via R50, and will revert to a low speed of approximately 500KHz, with proper component values, when the WAIT line B1 is brought low.

RESET is brought in on a control connector at NC3. Non-maskable interrupts (NMI) and interrupt requests (IRQ) are brought in on bus lines B2 and B3. The master system clock signal $\emptyset 2_{out}$ is buffered through 7417 to bus connection B42. This signal provides the master timing for all accessory boards. The data lines in the microprocessor are brought out through a set of 8T26 buffers whose direction is controlled through external data direction (DD) line B4. Under normal circumstances, the 6502 is transmitting data onto the system bus. When an external board decides that a read operation is present, it will bring the data direction (DD) line low and pass its data back to the processor. The PROMs and ROMs on a 500 board are connected directly to the microprocessor's data bus before the 8T26s. The 16 address lines, which select the device to receive or output data to the processor, are buffered via 7417s at IC-F1, IC-C1, and IC-C2. These are high-power open-collector bus drivers which are capable of sinking 40ma, or approximately 16 TTL loads. The board has provisions for pullup terminating resistors on board for these drivers. These resistors R34 through R48 must be present on the board if a backplane board is not present in the system. If the backplane board is used, at all times it is recommended that these pullup resistors be placed on the backplane board instead, as per App Note #2. All circuitry in diagram 1 must be present for any practical use of the 500 board.

RAM Implementation. (diagram 3)

The Model 500 board can have from 0 to 4K of onboard RAM using popular 2102-type memories. These memories must be of the "0"-data-hold time or A-type chips. Parts such as the 2102 LFPC, or P2102AL are excellent choices for use on the board. Since the 2102 is a 1K x 1 part, the board must have 8, 16, 24, or 32 chips for 1K, 2K, 3K, or 4K bytes of memory on board. These RAM chips will be placed at IC locations D1 to D16 and E1 to E16. When any RAMs are placed on the board, the additional circuitry shown on this diagram must be present. The upper address bits A15 through A10 are used to decode the address for the 4K of RAM and to further decode the 4K into 1K segments. The board is laid out for RAM to be present at 0 to 0FFF. However, inverters and convenient cut and jumper points are present on the board so that the RAM memory can be set at another 4K boundary. This circuitry is a set of four inverters on A12 through A15 on 7420 at IC-F3. The output of IC-F3 is a memory enable signal gated with A11 and A10 as a two- to four-line decoder, and Ø2·VMA which is a master timing signal to provide the low true chip enables for each block of eight 2102 memories. The board enable signal along with R/W and Ø2·VMA are gates to produce a data direction signal which changes the direction of the 8T26 buffers on the data bus to the 2102s, and also changes the system data direction (DD) line B4 from processor outputing data to processor listening. The WAIT diode D10 is optional, and only necessary when slow memory is used with a high clock speed system. This configuration for memory allows the 500 board to be used as a general-purpose memory board, i.e., additional 500s can be populated with just the components shown in diagram 3 as conventional 4K RAM boards. This feature, in itself, offers no advantage over our standard 420 memory board, but, if other features of the 500 board are desired such as the ACIA, ROMs, or PROMs, then this is an attractive alternative to the 420 board for additional 4K RAM when desired.

PROM Implementation (diagram 4)

The 500 CPU board can accept up to three 1702-type 256-byte EPROMs. The board is configured for several different options used in a wide variety of OSI products. This diagram shows address decoding for the PROMs. The 1702 PROMs' address lines are directly on the system address bus. The data lines are in on the internal data bus directly connected to the 6502 processor. The chips require +5 and -9 power connections. The upper six address bits for FXXX are generated by IC-F6 and provide the PROM enables which are also utilized for enabling the ACIA. The 7420s, IC-B3, B4, and B5, along with the inverted and non-inverted A9 and A8 address signals provide a two- to four-line decoder, gated by Ø2·VMA and R/W. This generates low true chip enables for an ACIA at FCXX and chip enables for 1702 devices at FDXX, FEXX, and FFXX. 1702 devices are protected against attempts to write into PROM, by being disabled during write operations. The 1702 located at FEXX can be set to be not completely decoded so that it occupies 512 words at FEXX and FFXX via IC-B5.

Part of IC-B5 generates a data direction (DD) signal which would be utilized only if these 1702 devices and/or the ACIA were put on accessory boards. Under normal circumstances, when the 6502 is on a 500 board with these components, data direction diode D3 must be omitted. The WAIT diode D8 is optional, and is only to be used when the processor is operated above 1MHz in normal mode, or if slow 1702 devices are used. Ohio Scientific normally supplies ultra-fast 3702 T-1 1702-type devices capable of operating with 6502s at 1MHz clock speed.

The three 1702 devices can be configured for many standard OSI configurations, as stated above. By not cutting jumpers K1 and K2, and by not adding J4, a conventional 65A or 65V PROM Monitor can be placed at IC-A5. This will allow the 500 board to function as the older 400 board. If a Floppy Disk Bootstrap is to be used in a system, then K1 is cut, J4 and J3 are installed, and the Floppy Disk Bootstrap is installed at IC-A6. This will then provide Floppy Disk Bootstrap operation in addition to the Monitor PROMs present.

If the board is used in conjunction with 8K BASIC ROMs, it will then require a serial-based or video-based support PROM. If either of these PROMs is the only PROM present in the system, it will be installed just as a 65A or 65V PROM. If these PROMs are desired in conjunction with a 65A or 65V PROM so that the user has access to machine code, the BASIC support PROMs must be installed at IC-A6 just as the Floppy Disk Bootstrap PROM would be.

Switch 1 can be installed so that the user can simultaneously install an 8K BASIC serial support PROM and BASIC video support PROM and select between them by placing these PROMs at IC-A5 and IC-A6. Cut K2 must be made and a switch installed at SW-1. Ohio Scientific is also planning to offer an expanded PROM Monitor set which makes use of the extended memory or memory management. This two-PROM set would replace a 65A or 65V PROM and must be placed at IC-A5 and IC-A4, and can be used with or without a Floppy Disk Bootstrap PROM or BASIC Support PROMs at IC-A6. Pay careful attention to the assembly instruction for the specific configuration you desire when installing these PROMs, as it can be confusing. All the parts in diagram 4 should normally be installed on board for any conventional application.

ROM Implementation (diagrams 5 & 6)

This diagram shows the decoding circuitry and pinouts for the 8K BASIC ROMs or other possible ROMs that can be utilized in the system. The board is laid out to accept our standard BASIC ROM set which comes in four Signetics 2616-type ROMs which have the same pinout as the Synertek or Intel 2316B PROMs. The typical ROM pinout is shown at the top of diagram 5. The address lines are directly connected to the system address bus, and the data lines to the processor. The ROMs are hard-wired at A0XX, A8XX, B0XX, and B8XX via inverters at IC-F9 and IC-C5 and the 7420 at IC-F8. Full decoding is implemented by 7420s at IC-C8 and IC-C7 by gating address signals with Ø2·VMA and R/W and presented as positive or negative chip enables. Additional data direction (DD) circuitry and D7 are provided when the board is used as an accessory board. Diode D7 must be omitted when the processor is present on the 500 board. Diodes D5 and D6 provide the WAIT function and are to be used only when the slow PROMs are implemented or if the machine is running with a fast clock.

As can be seen at the top of the diagram, ROM pins 18 through 22 are utilized for several different functions on different chips. Actually about twenty different chips share common pins everywhere except 18 and 22. The most popular ones are listed here. These pins and the choice of positive or negative logic chip enables can be programmed via two 16-pin sockets which are denoted as connector L2 and L3. The board is laid out to accept our standard ROM set without any foil cutting. However if another type of ROM, PROM, or EPROM is desired, it would be necessary to refer additionally to diagram 6, which shows some configurations for cutting foils and jumpering from pad to pad for other common parts.

2704s, 2708s and T.I. produced 2716s also require a -5 volt supply for operation. This supply must be populated as per the schematics at the lower portion of diagram 6. 2704s and 2708s also require a +12 supply, available in all Challengers from OSI as bus connection B23. Also note that if one is using

PROMs, ROMs, and EPROMs with less than 2K bytes of storage, there will be gaps in the address space. For example, in 2708s, there will be memory present from A000 to A3FF, and none from A400 to A7FF. This is because these locations are hardwired for four 2K x 8 ROMs starting at A000 and ending at BFFF. This should present no problem in any normal applications of the board.

Components in diagram 5 need only be populated when ROMs or user PROMs will be utilized.

Serial Interface (diagram 7)

The Model 500 has provisions for an ACIA-based serial interface with a standard 20ma current loop or RS-232 I/O. The interface utilizes a 555 baud rate clock which can function from 110 baud to 9600 baud. The ACIA decoding is shown in diagram 4. The board has provisions for both 20ma current loop and RS-232 current loop to populated simultaneously. Both current loop outputs can be simultaneously connected. However, only one input can be connected at a time. This is selected by two jumpers at the L1 connector IC-B1. The L1 connector has all critical signals present on it so that it can be used in conjunction with the 16-pin ribbon cable for convenient connection instead of the control connector at the top of the PC board. The 555 clock circuit has provisions for five capacitors which can be jumpered at J5. Selection of the capacitor, along with potentiometer R51, allows selection of baud rates from 110 to 9600. Jumpers K16 and K15, along with a tap at the L1 connector pin 10, allows utilization of an external clock. It is recommended that an external clock be used when a captive terminal is in operation. That is, if a terminal such as a MicroTerm ACT-I is intended to be used with the system at all times, then it would be advisable to pick off the UART clock signal in the MicroTerm ACT-I and route it to the 6850 ACIA via this connector. This will eliminate the possibility of any baud rate mismatch. The ability to have separate receive and transmit clocks allows the 6850 ACIA to be interfaced with the SW Tech Products AC-30 Cassette Interface. The 555 clock would then be used to transmit only, and the clock circuit in the Audio Cassette Interface would be used as a receiver clock. This option can also be used in multiprocessor configurations, where the transmitting processor provides the clock for the receiver, again to eliminate baud rate problems.

The RS-232 interfaces are for RS-232C only. They will not function with the old and seldom used RS-232B specifications. The 20ma current loop interface is specifically for use with the ASR-33 teletype. It has no common ground, and cannot be used with terminals requiring a common ground on input and output. It is recommended that the RS-232 be used when the user has a choice between the communication modes in his terminal.

The 6850 ACIA has several subtle features, e.g., signal lines which can be connected to modems. If the user anticipates any use such as this, it is recommended that he read the Motorola 6800 Family Manual which has a full description of the function of the ACIA. This serial port is located at FCXX and is supported as a control port in all OSI software. This port is also assumed to be the control console when used in conjunction with any OSI Disk Operating System if a serial PROM Monitor is present in the system. If a serial port is not needed, all of diagram 7 can be omitted from the PC board.

VII PIA Port (diagram 8)

The Model 500 can optionally have a 6820-based 16-line parallel I/O port, which is normally located at F7XX via a decoded circuit based on a 7430 at IC-F7. Two of the PIA output lines can optionally be routed back through 7417 buffers

to provide two additional address lines, A16 and A17, which will expand the addressable memory spaces from 65K to 256K. This feature is supported by a dual PROM set which allows multiple users on a system as well as other real-time interrupt-driven operations. For a more detailed explanation on the use of the PIA-based interface, please consult the Motorola 6800 Family's specification manual on the 6820. If the PIA interface is not required, all of diagram 8 can be omitted.

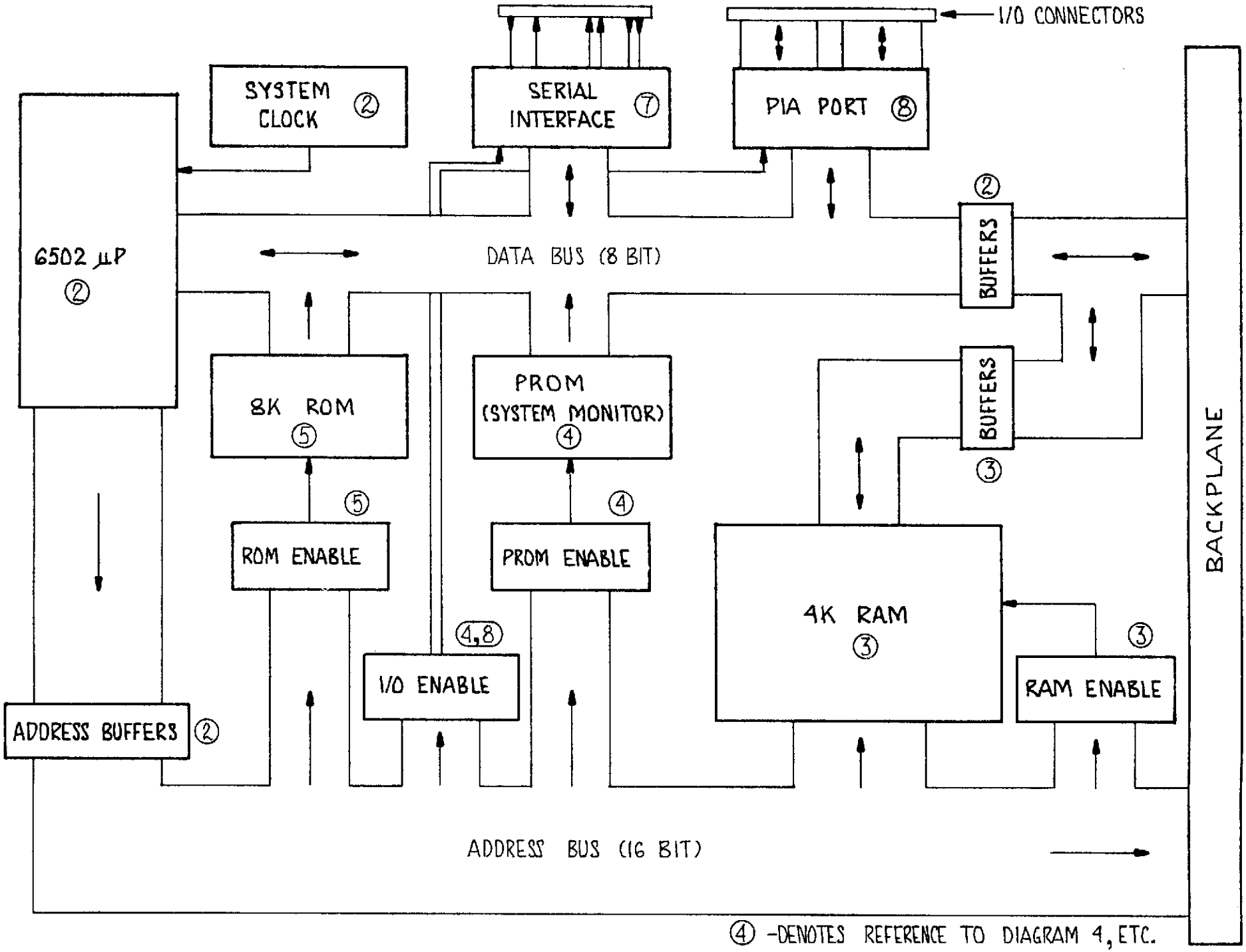


DIAGRAM 1 - SYSTEM OVERVIEW

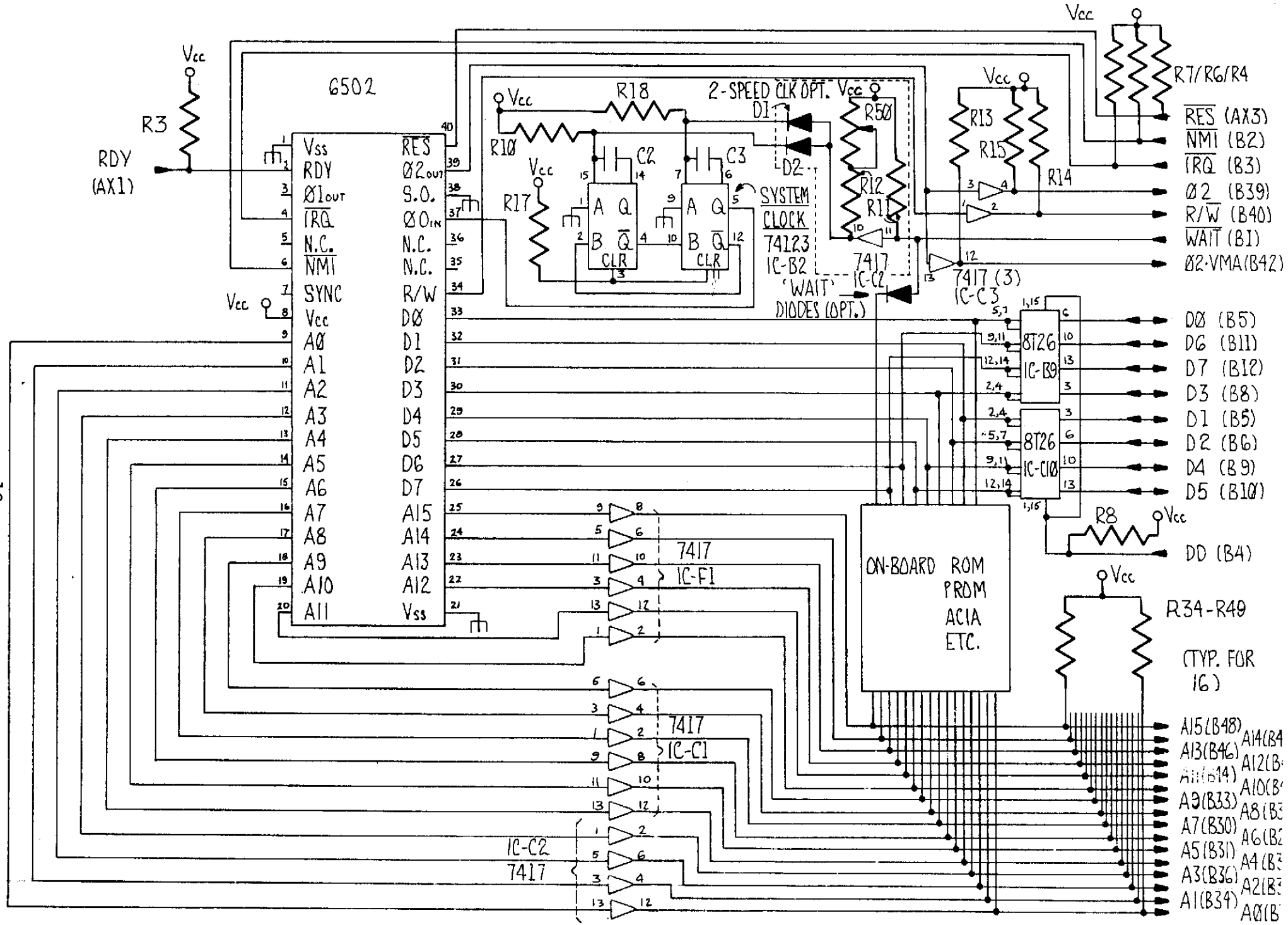


DIAGRAM 2 - MICROPROCESSOR, CLOCK, ADDRESS AND DATA BUS

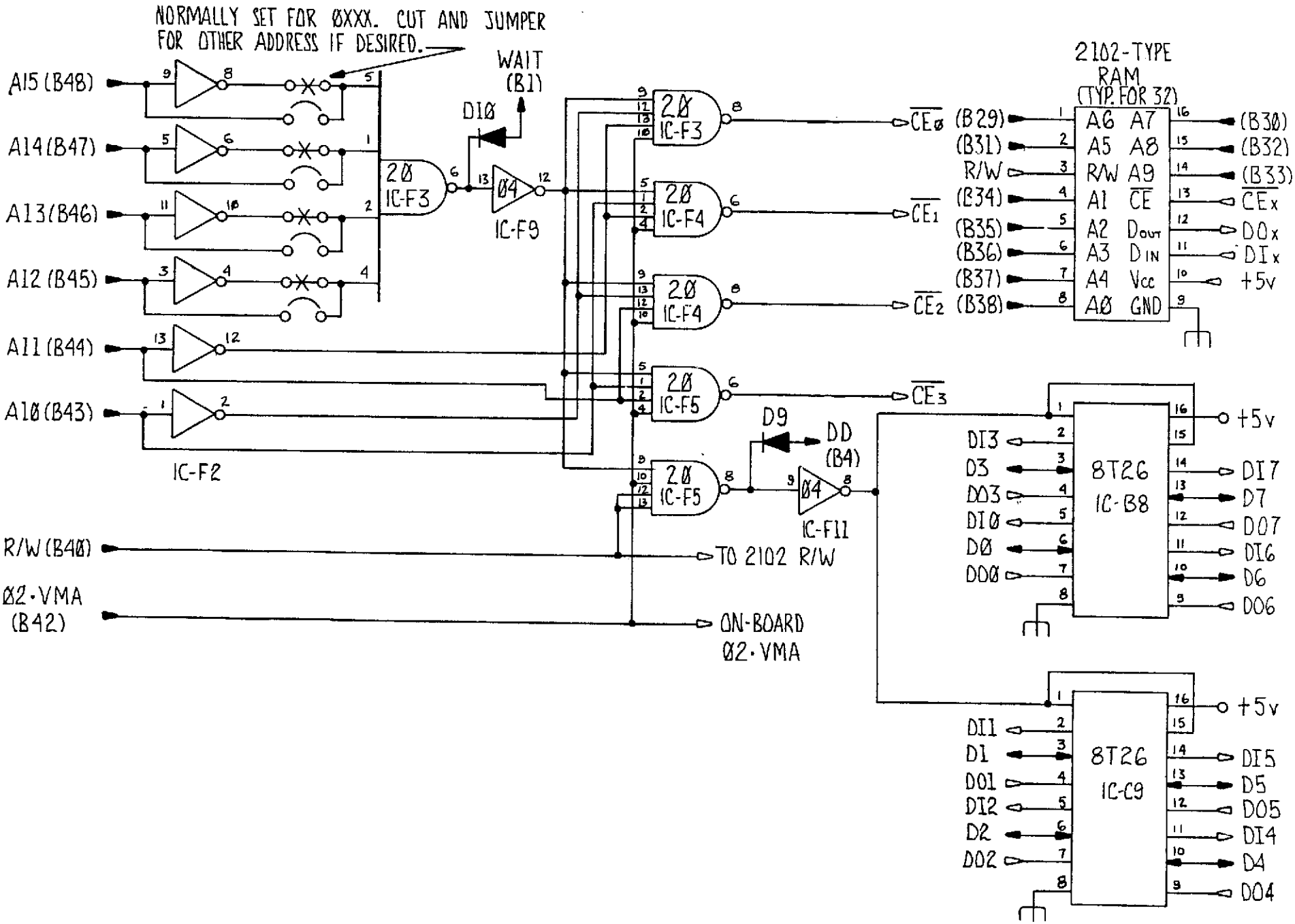


DIAGRAM 3- RAM IMPLEMENTATION

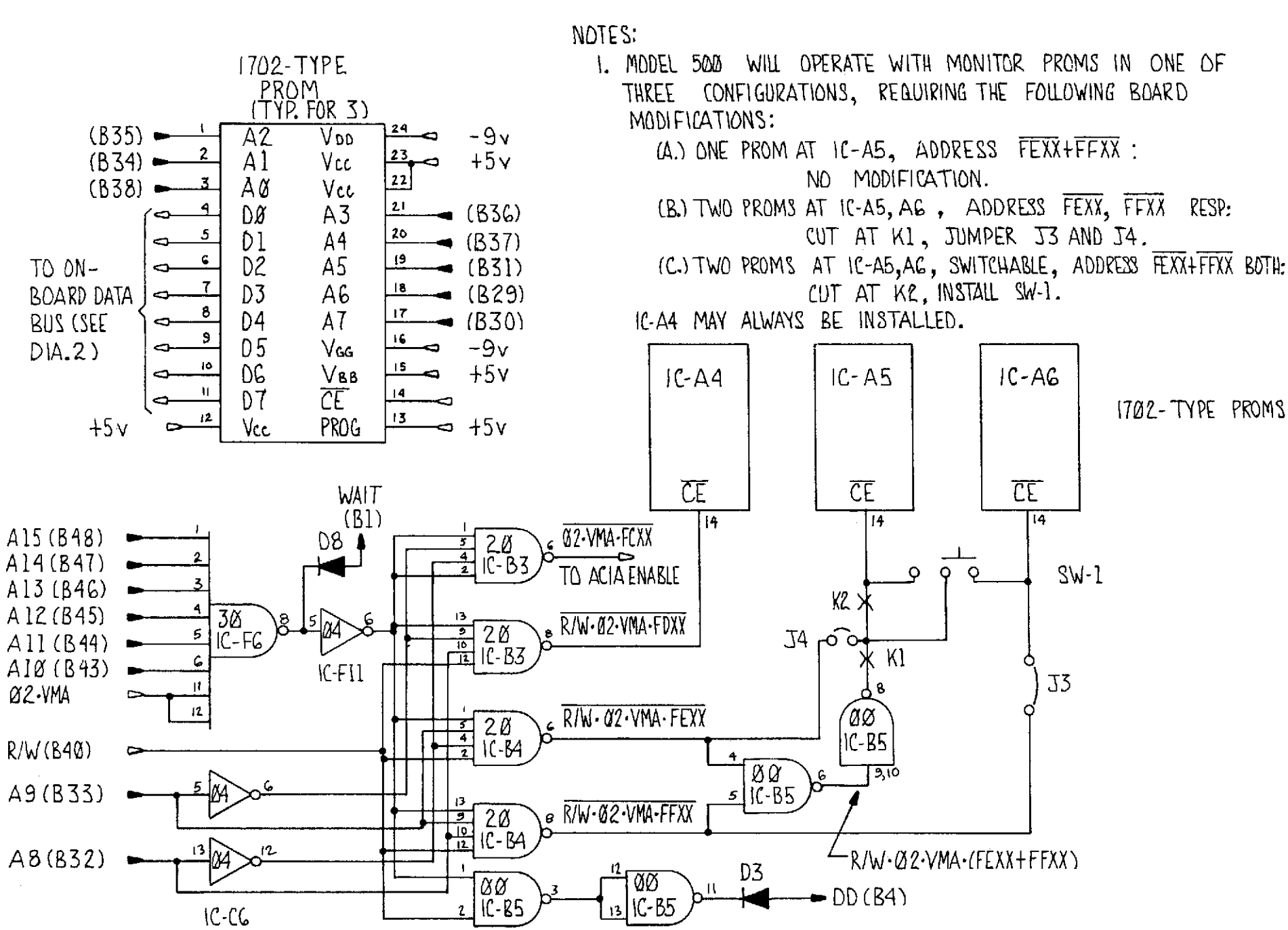
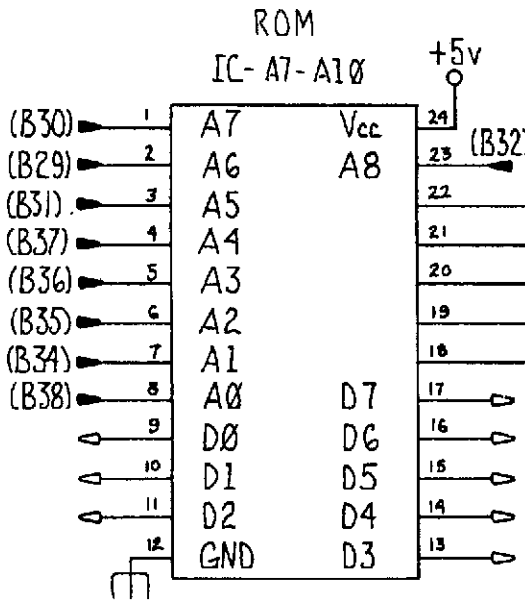


DIAGRAM 4- 1702-TYPE PROM IMPLEMENTATION



SYNERTEK SY2316B	INTEL 2704	INTEL 2708	INTEL 2716	TI 2716	INTEL 2316E
A9	GND	A9	A9	A9	A9
P	-5v	-5v	+5v	-5v	P
CE X	$\overline{CEX}$	$\overline{CEX}$	$\overline{CEX}$	A10	$\overline{CEX}$
A10	+12v	+12v	A10	+12v	A10
P	GND	GND	GND	$\overline{CEX}$	P

D0-D7:
TO ON-BOARD
DATA BUS
(SEE DIA.2)

NOTES:

1. P = CONNECTION TO +5v. (PULLUP)
2. BOARD NORMALLY SET FOR SY2316B. SEE DIA. 6 FOR MODIFICATIONS FOR OTHER CHIPS.

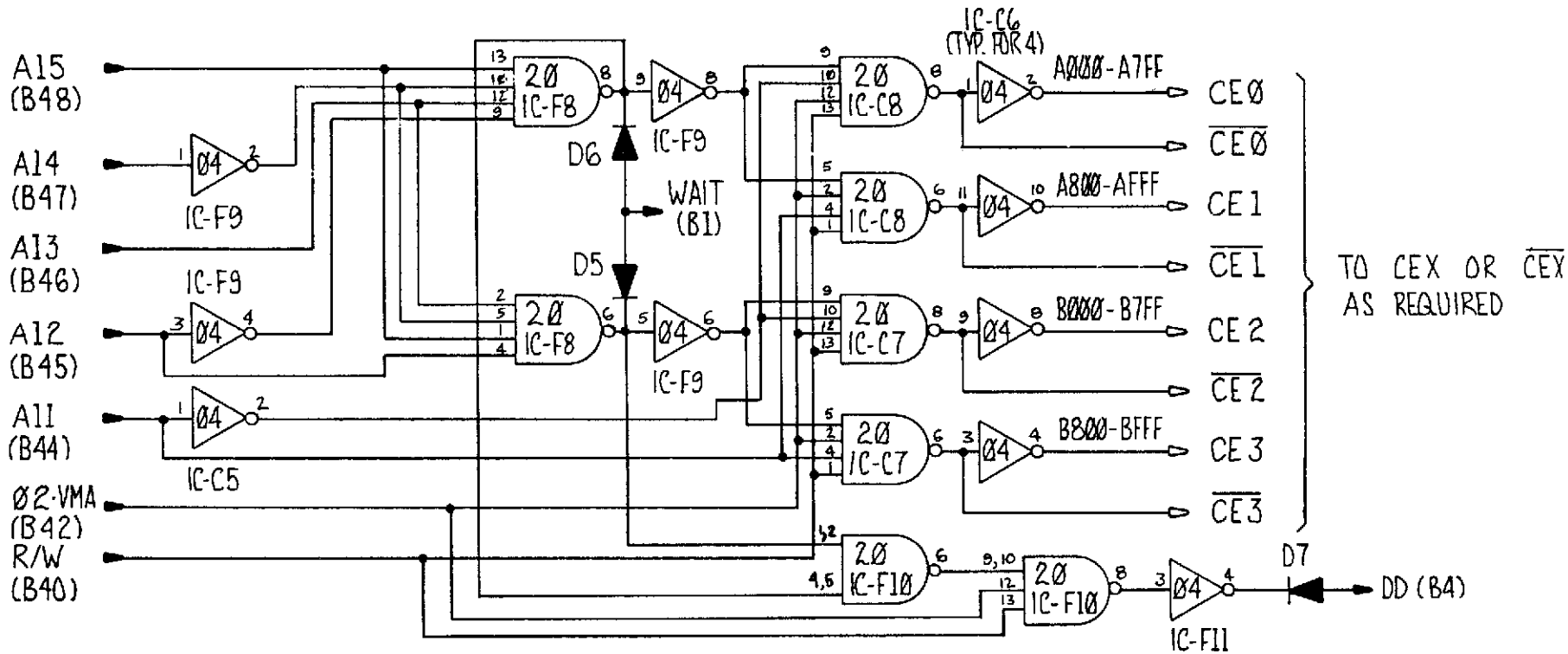
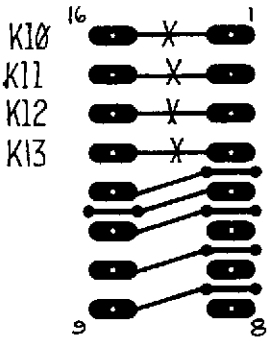


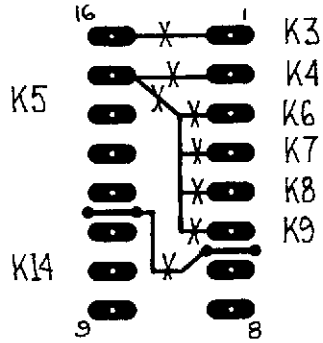
DIAGRAM 5- ROM IMPLEMENTATION (8K)

SYNERTEK SY2316B	INTEL 2704	INTEL 2708	INTEL 2716	TI 2716	INTEL 2316E
CUT	CUT	CUT	CUT	CUT	CUT
NONE REQ'D.	K-3 K-4 K-5 K-10 K-11 K-12 K-13 K-14	K-3 K-4 K-5 K-10 K-11 K-12 K-13	K-5 K-10 K-11 K-12 K-13	K-3 K-4 K-6 K-7 K-8 K-9 K-10 K-11 K-12 K-13	K-10 K-11 K-12 K-13
JUMPER	JUMPER	JUMPER	JUMPER	JUMPER	JUMPER
NONE REQ'D.	L2 p.7-p.6 p.8-p.1 p.9-p.2 L3 p.8-p.7 p.9-p.4 p.10-p.3 p.11-p.2 p.12-p.1	L2 p.7-p.6 p.8-p.1 p.9-p.2 L3 p.9-p.4 p.10-p.3 p.11-p.2 p.12-p.1	L2 p.7-p.6 L3 p.5-p.1 p.5-p.2 p.5-p.3 p.5-p.4	L2 p.8-p.1 p.9-p.2 p.11-p.6 p.12-p.5 p.13-p.4 p.14-p.3 L3 p.5-p.1 p.5-p.2 p.5-p.3 p.5-p.4	L3 p.9-p.4 p.10-p.3 p.11-p.2 p.12-p.1

NOTE: L3 p.9-p.4 means jumper pin 9 to pin 4 of connector L3, etc.



CONN. L-3



CONN. L2

(ABOVE) CONNECTORS L2 AND L3 SHOWING CUT POINTS. VIEW FROM REAR OF BOARD.

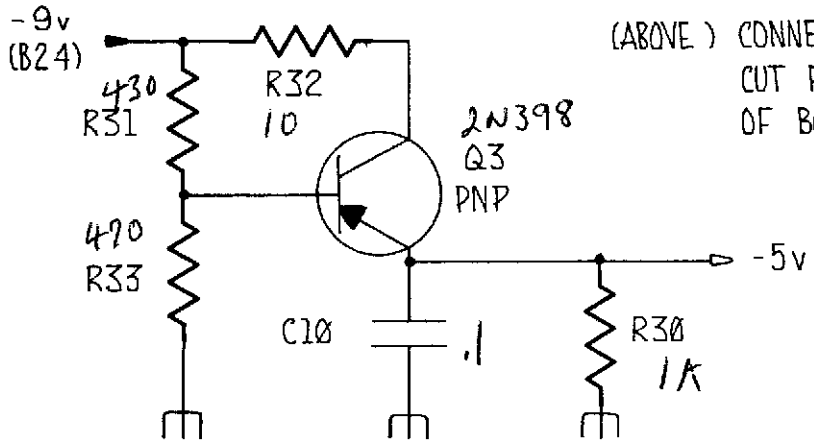


DIAGRAM 6- ROM JUMPER CONFIGURATION AND -5v POWER

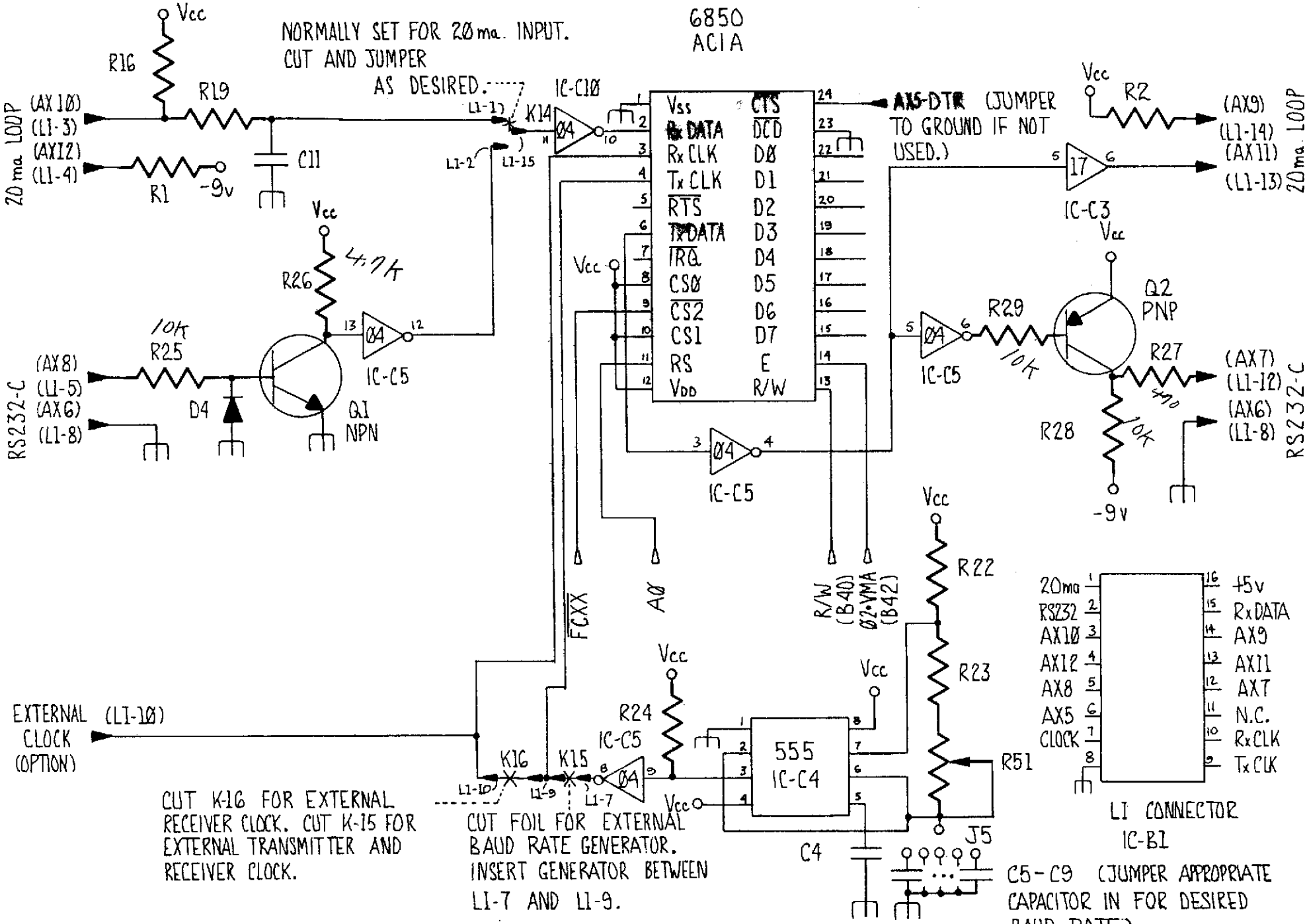
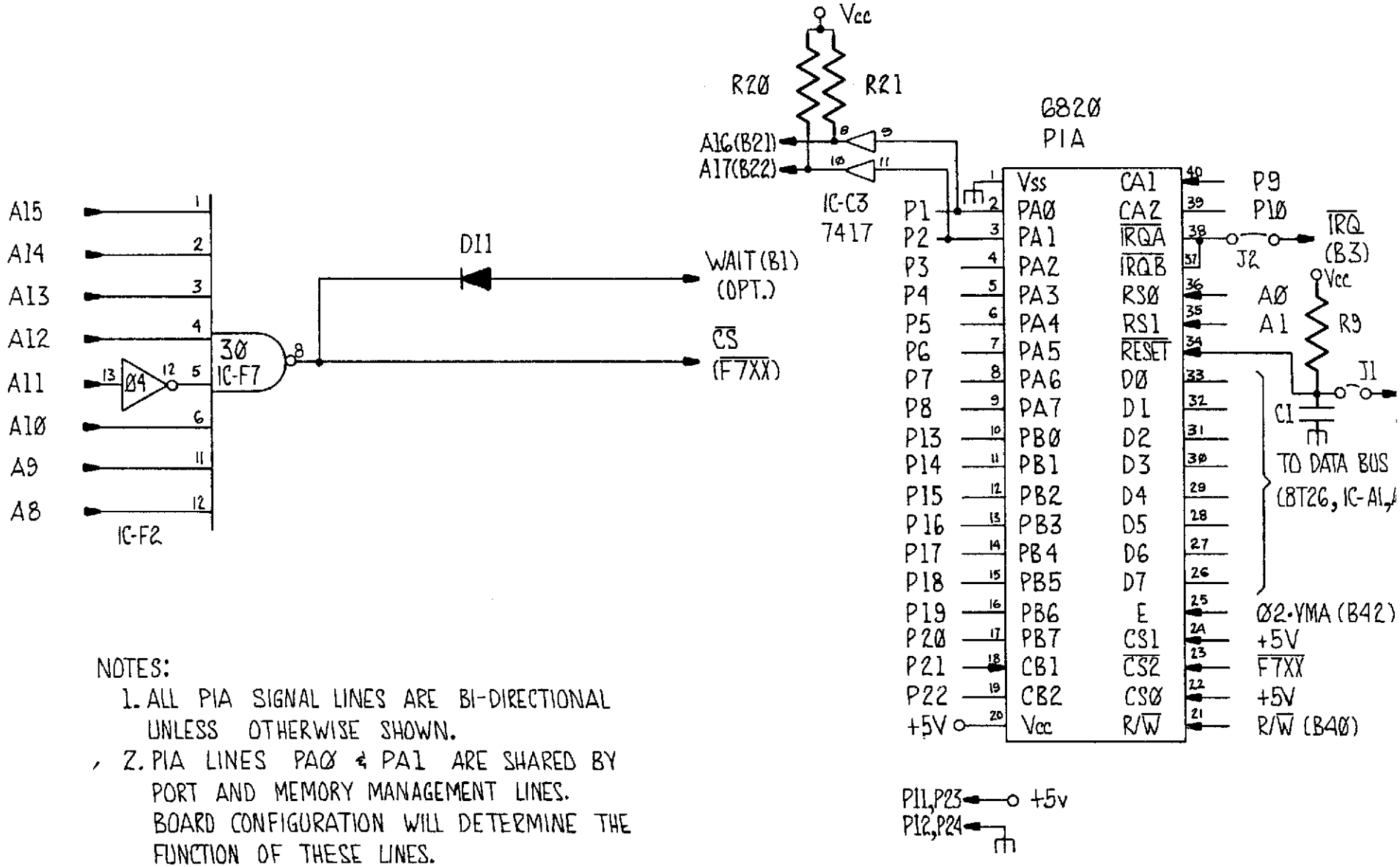


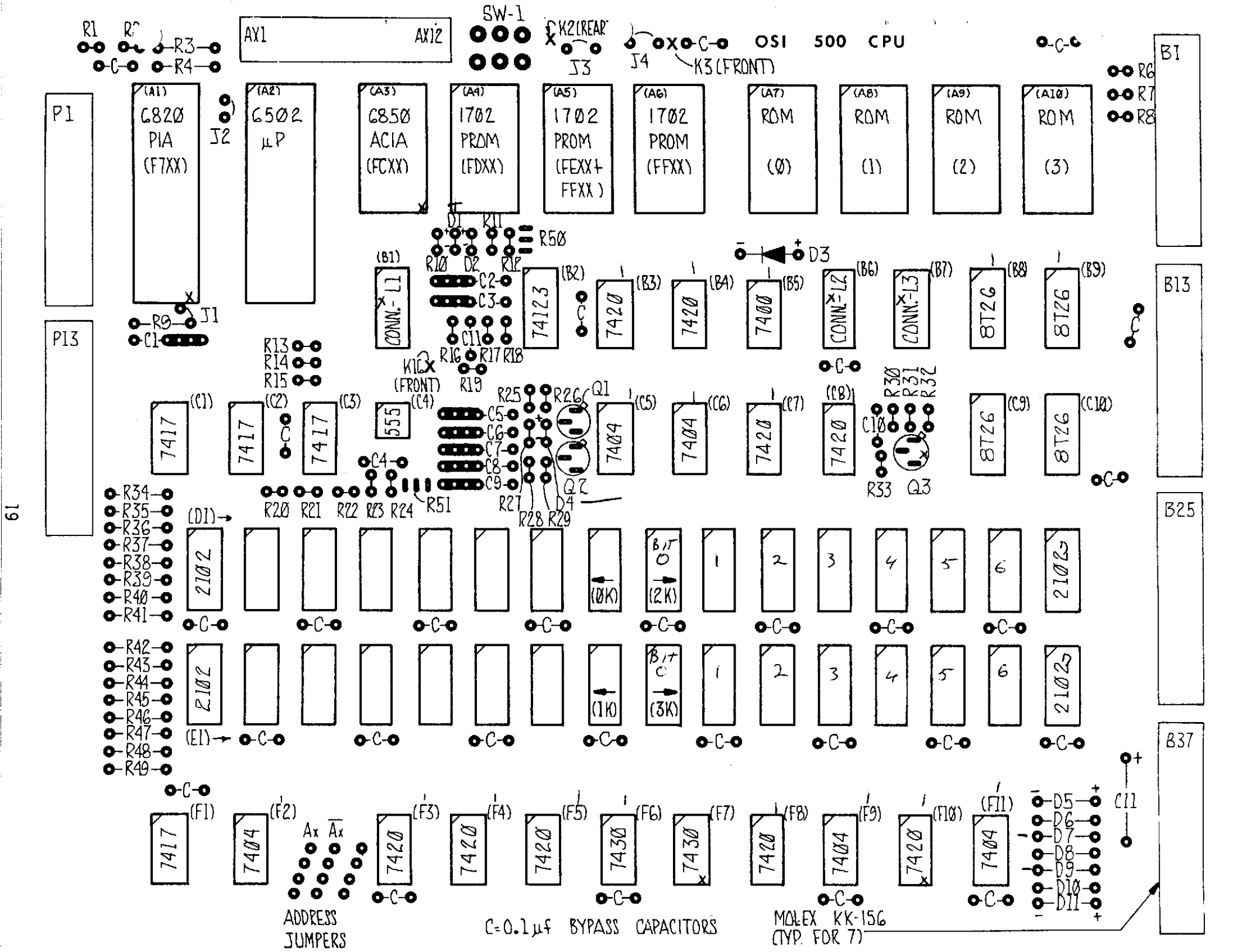
DIAGRAM 7- SERIAL INTERFACE



NOTES:

1. ALL PIA SIGNAL LINES ARE BI-DIRECTIONAL UNLESS OTHERWISE SHOWN.
2. PIA LINES PA0 & PA1 ARE SHARED BY PORT AND MEMORY MANAGEMENT LINES. BOARD CONFIGURATION WILL DETERMINE THE FUNCTION OF THESE LINES.

DIAGRAM 8- PIA PORT


OSI 500 CPU
AX1
AX2
SW-1
K2 (REAR)
J3
J4
K3 (FRONT)
P1
P13
B1
B13
B25
B37
(A1) 6820 PIA (F7XX)
(A2) 6502 µP
(A3) 6850 ACIA (FCXX)
(A4) 1702 PROM (FDXX)
(A5) 1702 PROM (FEXX + FFXX)
(A6) 1702 PROM (FFXX)
(A7) ROM (0)
(A8) ROM (1)
(A9) ROM (2)
(A10) ROM (3)
J1
J2
R1
R2
R3
R4
R5
R6
R7
R8
R9
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
R10
R11
R12
R13
R14
R15
R16
R17
R18
R19
R20
R21
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R32
R33
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
R45
R46
R47
R48
R49
R50
R51
Q1
Q2
Q3
K1 (FRONT)
CONN.-L1
CONN.-L2
CONN.-L3
74123
7420
7400
8T26
7417
555
7404
7430
2102
(0K)
(1K)
(2K)
(3K)
BIT 0
BIT 1
(B1)
(B2)
(B3)
(B4)
(B5)
(B6)
(B7)
(B8)
(B9)
(B10)
(C1)
(C2)
(C3)
(C4)
(C5)
(C6)
(C7)
(C8)
(C9)
(C10)
(D1)
(E1)
(F1)
(F2)
(F3)
(F4)
(F5)
(F6)
(F7)
(F8)
(F9)
(F10)
(F11)
Ax
Ax
ADDRESS JUMPERS
C=0.1µf BYPASS CAPACITORS
MOLEX KK-156 (TYP. FOR 7)
61

Part III. Assembly

A. ADDITIONAL COMPONENTS

Besides the 500 Board itself, some additional components will be needed to complete the system, depending on whether you are building a serial or video system. These are:

1. Power supply--+5V @ 2A
   -9V @ 500ma
   +12V (optional for some system configurations)

The current ratings are for a fully-populated Model 500 only. Any accessory boards will increase the power requirements. For a list of system boards which require +12V, consult the full-line catalog.

2. Model 480 Backplane (optional)--use this if accessory boards will be added to the system.

3. Model 440 Video Board (video systems)-- provides CRT terminal functions when used with 4, below. Consult full-line catalog for detailed specifications.

4. Keyboard and monitor (video system only)--The keyboard must be a seven-bit high-true ASCII encoded with either high- or low-true strobe. A television set equipped with an RF converter can be used as a monitor, but for sharpest display and highest resolution, a commercial monitor should be used. A color television or monitor will be used if the 440 color option is installed.

Ohio Scientific supplies monitors and a keyboard for use with video systems. Consult the full-line catalog for prices.

5. Serial terminal (serial systems only)--The Model 500 serial interface will support terminals at baud rates from 110 to 4800 baud, including teletypes and CRT terminals.

6. Reset switch--use an SPST momentary contact switch.

7. Enclosure--The system should be enclosed in an RF-shielded metal case. This item is supplied by the user.

B. TEST EQUIPMENT

The following test equipment should be available for setup and troubleshooting the system:

1. VOM--The voltmeter will be used to check the power grid on the board. The ohmmeter is used to check for continuity of foil runs, and for shorts between runs. An inexpensive VOM is adequate.

2. Oscilloscope--A good quality service or lab scope with a 10X probe is essential. For best results, the bandwidth should be at least 15MHz. It should have triggered sweep. If it has a calibrated time base, it can be used instead of a frequency meter to set the system clock frequency and the baud rate clock.

3. Frequency Meter (optional)--This is used to set the system clock frequency and the baud rate clock. An oscilloscope with a calibrated time base may be used instead.

4. Logic Probe (optional)--A minimal TTL-level logic probe is shown in Appendix III. This will indicate circuit activity under static and some dynamic conditions. If a more elaborate logic probe is available, it should be used, of course.

5. TTL Data Book (optional)--If you do not already have one, you can get one directly from most of the major chip manufacturers. Radio Shack also sells one which retails for under five dollars.

6. Additional documentation is available from MOS Technology, Inc., 950 Rittenhouse Road, Norristown Pa. 19401. The cost of their Hardware Manual and Programming Manual is five dollars each.

If you anticipate implementing the optional PIA port, obtain a data sheet on the 6820 from your local distributor.

C. PRE-ASSEMBLY INSTRUCTIONS

Before you begin assembly, you should first read the entire manual thoroughly. For example, the information in Part II, Theory of Operations, is invaluable in troubleshooting. Part IV, Bringing up the System, will explain the features and functions of a completed operational system. It will provide the rationale for the order of the construction steps and for the testing procedures.

The Model 500 CPU is very complex; assembly and troubleshooting are very intricate procedures. Particularly in troubleshooting, we assume that you have some previous electronics experience. In each testing section guidelines are given to correct problems you may encounter, but they are by no means exhaustive. You may need to refer to the schematics and the Theory of Operation to track down a particular problem.

The Model 500 is extremely versatile. There are many optional configurations to choose from. For example, you can make it accommodate about a dozen different ROMs by simply reconfiguring a jumper area. All such options are mentioned in the schematics. However, only a few of the most popular ones are described in the assembly instructions. The options not covered are relatively simple, and should be easy to implement from the schematics.

If you are building a video system, we recommend constructing the video board first. If possible, test it with another CPU which is known to be working. It is difficult to bring up a video board and CPU simultaneously, because if a problem occurs, there is no easy way to determine which of the boards is causing it. However, this can be done if necessary. First, follow the Model 440 manual to the point where you get a good, stable display of random characters on the screen. Then construct the Model 500 Board. The assembly instructions outline the procedure of testing both boards simultaneously. Also, the backplane should be constructed at this time. We strongly recommend socketing all parts. As a minimum, the Monitor PROMs (IC-A4,-A5,-A6), BASIC ROMs (IC-A7,-A8,-A9,-A10), and 2102 RAMs should be socketed.

The first and most important construction step is to inspect the board thoroughly!!! Do not take any shortcuts here. As indicated above, the Model 500 is a very dense board. Narrow traces and close spacings sometimes result in runs or foil bridges between runs. These can be seen most easily by backlighting the board with a strong source, such as a desk lamp, and by inspecting both sides of the board carefully. Foil bridges can be scratched out with a sharp razor; open runs can be touched up with a soldering iron. Be thorough. A few extra minutes now may save an hour of troubleshooting and a blown part later.

Consult the list of errata in Appendix II. Several corrections to the printed circuit board may be necessary, depending on the revision number of the board. These are most easily done before any parts are soldered in.

Use a 25-watt fine-tipped soldering iron and 60/40 rosin core solder. Do not apply excessive heat to the board, as this may cause foil to lift from the epoxy base. Excessive heating may also damage integrated circuits. MOS devices are sensitive to static charges, so do not remove these from their foam carrier until they are ready to

install. Do not touch the pins with your hand.

D. ADDRESS DECODING, ADDRESS AND DATA BUFFERS

1. Install resistors R3, R4, R6, R7, R8, R13, R14, R15. Resistors R13-R15, R34-R49 are bus pullups and may be placed either on the Model 500 or on the backplane (we recommend placing them on the Model 500). Install them at this time. If the board will be used with a backplane, install Molex connectors along the right edge of the board. Install a Molex connector in the top left corner of the board (serial interface connector).

2. Integrated Circuits:

BUFFERS	IC-C1	7417
	IC-C2	7417
	IC-C3	7417
	IC-F1	7417
	IC-B8	8T26
	IC-B9	8T26
	IC-C9	8T26
	IC-C10	8T26
RAM DECODER (opt.)	IC-F2	7404
	IC-F9	7404
	IC-F11	7404
	IC-F3	7420
	IC-F4	7420
	IC-F5	7420
PROM DECODER	IC-B5	7400
	IC-C6	7404
	IC-F11	7404
	IC-B3	7420
	IC-B4	7420
	IC-F6	7430
ROM DECODER (opt.)	IC-C5	7404
	IC-C6	7404
	IC-F9	7404
	IC-F11	7404
	IC-C7	7420
	IC-C8	7420
	IC-F8	7420
	IC-F10	7420
PIA DECODER (opt.)	IC-F2	7404
	IC-F7	7430

3. Wait and Data Direction diodes. If the RAM is to installed, install Data Direction diode D9. For clock speeds above 1MHz install Wait diode D10.

For each of the following modules, install the Data Direction diode if the Model 500 is to be used as an accessory, that is, when it is not the system CPU. Install the Wait diode for a given module if the system clock is above 1MHz.

	DD	WAIT
PROM/ACIA	D3	D8
ROM	D7	D5, D6
PIA	--	D11

Note that the PIA may not be used as an accessory to an off-board CPU.

4. Capacitors. Install bypass capacitors near IC-A1, A10, B3, B9, C2, C8, C10, F1, F3, F6, F9, F11. Install capacitor C11.

5. Testing.

a) Verify operation of the power supplies by powering up and measuring the voltages with a VOM. Measure +5V to ground, -9V to ground, and +5V to -9V. If all is well, connect power supply to the board. Good practice dictates that the power be turned off while the board is being connected to the power supply and plugged into the backplane; this is because some components can be damaged if either of the power supply voltages is applied before the other. Always make the mechanical connections first, them simultaneously apply power to the supplies. Measure both voltages at the bus connectors. A folded-back supply indicates a short somewhere on the board. Power down the board and visually inspect for shorts.

b) (Address Bus Checkout) This tests for the presence of all address bits of various points on the board, and for shorts between address bits. Refer to Diagram 2 for bus pinouts and microprocessor pinouts.

(1) Power up the board. With a test probe (logic probe or oscilloscope), test all bus points B29-B48 at the backplane connector. All lines should be high.

(2) Probe address bit A0 at the backplane connector. Now, ground A0 at the microprocessor socket. A0 should go low.

(3) With A0 still grounded, probe all other bus points B29-B48. These should still be high.

(4) Repeat steps (2) and (3) for A0-A15, R/W, 02, 02. VMA

(5) Refer to the schematics in Diagrams 3, 4, 5, 7, and 8 and selectively ground A0-A15, 02. VMA, R/W. Observe each at the following sockets:

Each of thirty-two 2102 RAMs
PROM: IC-A4, -A5, -A6
ROM: IC-A7, -A8, -A9, -A10
ACIA: IC-A3
PIA: IC-A1

This verifies that all addresses to these chips are connected and working correctly.

(6) If a failure occurs, it will be probably due to one of two reasons:

If it occurs at step (1), there is either a broken trace between the processor and the backplane connector or a faulty 7417 buffer. With the power off, use an ohmmeter to check the printed circuit trace for continuity. Check at several points along the trace to isolate the break. If this is not the problem, replace the 7417.

If failure occurs at steps (2), (3), or (5), there is probably a short between two adjacent traces. Carefully inspect the board along the trace in question. Remember to check branches of the trace which go to remote areas of the board. If a short has occurred, the 7417 may have been damaged and may need to be replaced.

c) (Data Bus Checkout) This section tests for the presence of all data bits at various points on the board, for shorts between data bits, and for functioning of the 8T26 buffers. Refer again to Diagram 2 for bus pinouts and microprocessor pinouts.

(1) Power up the board. With a test probe (logic probe or oscilloscope) test all bus points B5-B12. All lines should be low.

(2) Probe D0 at the backplane. Ground D0 at the microprocessor. D0 at the backplane should go high.

(3) With D0 still grounded, probe all other bus points at D0-D7. They should still be low.

(4) Repeat steps (2) and (3) for all other data bits.

(5) Ground backplane point B4 (Data Direction). Probe D0-D7 at the microprocessor. All lines should be low.

(6) Probe D0 at the microprocessor socket. Ground D0 at the backplane connector. D0 should go high.

(7) With D0 still grounded, probe all other data bits at the microprocessor. They should still be low.

(8) Repeat steps (6) and (7) for all other data bits.

(9) Refer to the schematics in Diagrams 3, 4, 5, 7, and 8 and selectively ground D0-D7. B4 should still be grounded. Probe to observe activity of each data bit at each of the following sockets:

Each of thirty-two 2102 RAMs
PROM: IC-A4, -A5, -A6
ROM: IC-A7, -A8, -A9, -A10
ACIA: IC-A3
PIA: IC-A1

(10) If a failure occurs, it will probably be due to one of several reasons:

(a) If it occurs at step (1), there is either a broken trace between the processor and the backplane, a faulty 8T26 buffer, or Data Direction line (B4) not pulled up. Follow the same procedure described in Address Bus Checkout, b).

(b) If a failure occurs in steps (2) or (3), there is probably a short between two adjacent traces. Follow the procedure in Address Bus Checkout, b).

(c) If a failure occurs at steps (5),(6),(7), or (9), the cause is probably as in (b), above. Also verify that B4 is grounded (step (5)), as this may be the source of the problem.

d) (Decoder Checkout) This section tests the operation of the various decoder sections by manually setting up addresses at the microprocessor socket and observing the resulting enable signal. Refer to the table on Page 48B and the schematics in Diagram 2.

At this point the inputs to the address buffers are not being loaded, so they will drift high. The address on the bus will be FFFF. To set up a different address, ground the appropriate address bits at the microprocessor socket. For example, to set up 00XX, ground bits A8-A15. The other bits may be high or low, since they are not decoded at this stage. Use this method in the following test procedure:

(1) Attach a logic probe or oscilloscope at the source pin. The enable should be at the inactive level.

(2) Using the above method, set up an address range. The enable should go to the active level.

(3) Set up an address outside the enable range. The enable should go to the inactive level.

(4) Repeat steps (2) and (3) for several addresses.

(5) Now, attach the logic probe or oscilloscope to the destination pin(s). Repeat steps (2) and (3) to verify circuit continuity between source and destination. Check all destination pins. Repeat this procedure for all sections being built.

(6) If a failure occurs, it will probably be due to one of the following reasons:

(a) If it occurs in steps (1), (2), or (3), there may be a break in an address line or a shorted address line to the decoder chip. It may be a shorted chip enable output, or a faulty chip in the decoder circuit. Refer to b), Address Bus Checkout, for remedies.

(b) If it occurs in step (5), it is probably a broken printed circuit trace. Refer again to b), above.

E. SERIAL INTERFACE AND SYSTEM CLOCK

1. Serial Clock (optional--for serial systems only). Install R22, R23, R24, R51, C4, C5-C9 (as needed; select for desired baud rates).

IC-C4	555
IC-C5	7404

Jumper in the appropriate capacitor C5-C9 for the desired baud rate. See table of capacitor values in Appendix V.

2. Testing. Connect an oscilloscope or frequency meter to connector LI-7. Adjust potentiometer R51 for a frequency sixteen times the desired baud rate. If the clock fails to operate at all, there is probably a foil short or solder bridge on the board. Alternatively, the 555 may be bad, or a resistor or capacitor of incorrect value may have been installed somewhere.

3. Serial Interface. You may install either the 20ma or the RS-232 interface, or both. However, only one input at a time may be jumpered into the circuit.

a) 20ma interface: Input--Install R1, R16, R19, C11
Output--Install R2

b) RS-232 interface: Input--Cut K14 (see Diagram 7), jumper LI-2 to LI-15. Install R25, R26, D4, Q1
Output--Install R27, R28, R29, Q2.

c) Install an ACIA at IC-A3. Jumper pin 24 to ground if DTR is not used (normally it will not be used). For systems operating above 1MHz, install Wait diode D8.

d) (optional) If Model 500 is used as an accessory board (i.e., the CPU is on some other board in the system, install diode D3.

4. Testing of the serial interface will be done under section D after the monitor PROMs are installed.

5. System Clock. Install R10, R17, R18, C2, C3. If the two speed option is desired, install R11, R12, R50, D1, D2. Install IC-B2, 74123.

6. Power up the board and, using an oscilloscope or frequency meter, measure the system clock frequency at the microprocessor socket, pin 37. It should be around 500 KHz. If the two-speed option has been installed, the frequency will be between 1MHz and 2MHz. R50 adjusts this frequency, which is normally set to 1MHz. Next, ground Wait at the backplane connector B1. The frequency should drop to about 500KHz.

7. If the clock fails to operate, there is probably a shorted or open foil, or a solder bridge. Inspect the board carefully. Alternatively, IC-B2 may be defective. Make sure that all resistors and capacitors are of the correct value.

F. RAM, PROM, MICROPROCESSOR, ROM, PIA

1. RAM. Install eight, sixteen, twenty-four, or thirty-two 2102-type RAMs in rows D and E. Fill in order from 0K to 3K, as shown on the parts overlay (Page 19). Install four bypass capacitors under each bank of eight 2102s installed.

2. PROM. Install a 65A (for serial systems) or 65V (for video

systems) at IC-A5. This part should be socketed.

3. Microprocessor. Install a 6502 at IC-A2.

4. Testing. This section tests system operation under the PROM Monitor.

a) Connect an SPST momentary contact switch between connector points AX2 and AX3. This is the reset switch. We recommend attaching the pair of wires from the switch to a male Molex connector. Cut the twelve-pin male connector to form a four-pin and an eight-pin connector. Attach the reset leads to the four-pin section and plug into the serial connector at the top left corner of the board.

b) If you have a serial terminal, refer to Diagram 7 and attach leads from the terminal to the appropriate pins on the eight-pin connector from step A. Plug into the serial connector.

c) Video Systems. Plug the Model 500 and the Model 440 Video Board into the backplane, and connect the keyboard and video monitor according to directions in the Model 440 Manual. Power up the system. When you momentarily depress the reset button, the video screen should clear except for six hexadecimal digits in the upper left corner. Turn to page 37 and run the demonstration program in that section.

d) If the system fails to operate, the cause may be either the Model 500 or the Model 440, or both. If the system fails to reset, first check the reset switch and connections to it. Also make sure that R3 and R4 are installed and of the correct value. Use a VOM to check for power and ground on the microprocessor and PROM. If the Model 440 has not been tested on a working system, it may not be functioning properly. Consult the 440 manual for troubleshooting procedures.

e) Serial Systems. With the reset switch and serial terminal connected, power up the system. Momentarily depress the reset switch. The terminal should output a carriage return--linefeed. Refer to page 31 for operation of the monitor.

f) If the system fails to operate, the baud rate may be slightly misadjusted. Depress the reset switch several times while rocking the baud rate potentiometer R51. For some setting of R51, you should get a carriage return--line feed. Make sure that the serial terminal is connected properly. If this fails, check the reset switch and connections to it. Also make sure that R3 and R4 are installed and of the correct value. Use a VOM to check for power and ground on the microprocessor,, PROM, and ACIA.

5. Additional PROMs (optional). For disk systems, install a 65-500F PROM at 1C-A6. For video systems with ROM BASIC, install a 500VB PROM at IC-A6. For serial systems with ROM BASIC, install a 500AB PROM at IC-A6.

If you install any PROM at IC-A6, make cut K1 and install jumper J4. Refer to Diagram 4.

6. BASIC ROMs (optional). Install the four BASIC ROMs in locations IC-A7 through IC-A10. The ROM marked BASIC 1 goes in IC-A7, BASIC 2 goes in IC-A8, etc.

7. Final testing.

a) (Disk only) Power up the system. Momentarily depress the reset button. The terminal (either serial or video) should respond with D/M? Proceed to Part IV of this manual.

b) BASIC only. Power up and reset the computer. The terminal (either serial or video) should respond with C/W/M? Proceed to Part IV of this manual.

c) If the system fails to operate, make sure you have installed the cut and jumper in step 5. Make sure the BASIC ROMs are in the correct order. Check power and ground to all PROMs and ROMs.

8. PIA (optional). The PIA is used either as a parallel I/O port or to control two memory management bits, A16 and A17.

a) If desired, install two Molex connectors along the left edge of the board. If desired, install R9-C1 for power on reset of the PIA. Otherwise install J1. Install R20 and R21.

b) Install the 6920 PIA at IC-A1.

c) Testing. Power up and reset the system. Try outputting to and inputting from the PIA, according to the 6820 manual.

Part IV. Bringing up the System

After the 500 CPU Board is assembled and tested (Part III), it is now capable of being used as the basis of a complete, operational computer system. This section explains how to bring up a 500-based serial or video system and describes the operation under the PROM Monitor and the use of BASIC ROMs.

Remember that the 500 CPU can be used in either serial or video form, with audio cassette or floppy disk, and with or without ROM BASIC. Your system will be configured for one of these versions. All possible versions are discussed here. To avoid confusion, keep in mind which version you have.

A. 500 BOARD AND SUPER-KIT POWER SUPPLY CONNECTIONS

The diagram on page 52 shows the right side of the Model 500 Board and gives information concerning power requirements and connectons for bus lines 24, 25, and 27. This bus line orientation is the same as the bus discussion on page 3. On 500 Board systems it will be necessary for you to connect well-regulated power supplies directly to the PC board via a mating Molex male connector or by direct solder connections. The power supplies utilized should preferably have both overcurrent and overvoltage foldback regulation. The -9V and the +5V power supply's ground should both be connected to B27. Be sure to use sixteen-gauge wire or heavier on the +5V power supply. Also make certain that the power supplies come up nearly together and go down together, that is, neither power supply voltage should be present for extended periods of time without the other power supply voltage. On video systems it will be necessary for you to plug the 500 PC Board into the backplane, usually at slot 1 in the computer. Power connections are usually made directly to the backplane board in the same fashion.

-9V to B24
+5V to B25
Ground to B27

For video systems, the +5V power consumption can be nearly 3amps. It must be stressed again that it is extremely important that you use well-regulated high quality power supplies. This will minimize the possibility of damaging any of the expensive computer circuitry in case of a malfunction.

B. INTERFACING THE CONTROL CONSOLE

There are two basic types of computer terminals utilized for communications with the machine. One type is a serial terminal. Examples of this are the popular ASR-33 Teletype, and CRT terminals such as the Lear Siegler ADM-3 or the Hazeltine 1500, and the DEC Writer LA-30. These devices communicate with the computer over a serial interface which is usually composed of three or four signal lines. Fairly elaborate interface circuitry is present at both the computer and the terminal to facilitate interface via a few lines. There are two basic types of serial interface: the RS-232C interface specification and the 20ma current loop specification. CRT terminals usually are configured for RS-232C whereas the Teletype and many DEC-Writers are configured for 20ma current loop. Additionally, terminals come at different print-out or baud rates. Baud rates on

terminals can vary from a slow 110 baud to 19,200 baud.

The other general class of computer interface is a video interface. This type of configuration has most of the terminal electronics built into the computer in the form of a video display board such as the Ohio Scientific Model 440B Video Display. The user must simply provide an ASCII parallel keyboard and a video monitor or closed circuit television for operation.

For either interface, connect an SPST momentary contact reset switch to the connector at the upper left of the board. Solder a pair of wires to a male Molex connector at points AX2 and AX3 (see Appendix VI) and bring them out to the switch on the front panel.

C. MODEL 500 BOARD SERIAL INTERFACE INSTRUCTIONS.

The Model 500 Board is capable of operating under RS-232 or 20ma current loop at 110, 300, 1200, 2400, or 4800 baud. If you specified the baud rate and configuration when you ordered the system from the factory, it should be configured as you requested. If you did not request a specific configuration, it will usually be delivered configured for RS-232 at 300 baud. The first step on your part is to find out which serial interface configuration (i.e., RS-232 or 20ma current loop) and which baud rate your terminal requires. We recommend the RS-232 interface and a baud rate of 2400 whenever a choice is possible, as is usually the case on CRT terminals. In conjunction with the discussion below, please refer to Appendix VI, which shows the upper left corner of the 500 Board.

Serial interface connections are made via the auxiliary connector along the top of the board. A Molex male connector has been provided to allow you to solder your own wiring to this connector. It will also be necessary for you to provide a momentary-action normally open reset switch to pin 2 and pin 3. This will be your system reset switch Pins 6,7, and 8 are for RS-232C. Pins 9 through 12 are for 20ma current loop. Only one configuration can be used at a time. The socket directly below the 6850 ACIA can be jumpered for either 20ma current loop or RS-232C. Contrary to the diagram, it may come from the factory jumpered for either 20ma current loop or RS-232. Inspect the PC board. If it is jumpered for RS-232, you may change it to 20ma current loop by jumpering pin 1 to pin 15 of the socket; on the other hand, 20ma current lop is changed to RS-232 by jumpering pin 2 to pin 15 of the socket.

Note: All Challenger systems require that their serial terminals be configured for full duplex operation with eight bits, no parity, and two stop bits.

On power-up it is possible to change the number of stop bits and parity under software control once the system is up and running by changing the ACIA status word. The status word is located at FC00.

D. RS-232 INTERFACE

Refer to Appendix 5 for RS-232 hookup connections.

E. 20ma CURRENT LOOP

The 20ma current loop of the Challenger Systems is configured specifically for the ASR-33 Teletype, which has four separate lines for interfacing. The Challenger 20ma current loop is an active loop which requires separate current returns for both receiver and transmitter, that is, it cannot be operated in the three-wire mode. It is extremely important that the user insure that his terminal is fully passive, that is, that the terminal does not provide the current source for the loops. Several Teletypes with modems have a high

voltage current source present in them which would destroy the current loop interface in the Challenger if connected. Be sure that your 20ma current loop device is configured to be passive. Rever to Diagram 7 for 20ma interface connections and the pictorial connections for Teletypes in Appendix 5. Once you have completed and double-checked the interface to your terminal, proceed with the system check-out using the 65A PROM Monitor on page 31.

F. MODEL 500 BOARD VIDEO INTERFACE INSTRUCTIONS

Video interfacing is composed of two parts: one connecting the video display, and one connecting the parallel keyboard. The video interface is accomplished by a Model 440B Video Interface Board.

A special dedicated video interface is incorporated on the Model 400 circuit board, which provides industry standard one volt peak-to-peak video output via an RCA phone jack. This jack is located on the 440B Video Board. The output of this phono jack can be directly connected to the input of any standard closed circuit video monitor such as those offered by Sanyo, GBC, Koyo, Panasonic, and others. The unit usually operates best when terminated by a high impedance load instead of a 75 ohm load. It may be necessary to provide some adjustments to the monitor, and this will be discussed later. It is also possible to modify some conventional television sets to be closed circuit receivers by directly injecting video into one of the video amplifier stages. We do not recommend this modification unless you are highly qualified or well versed in television circuitry. It is extremely important that you not attempt any such modificatons on a non-isolated or "hot chassis" television set. Interconnection between any portion of a "hot chassis" television set and the computer will cause severe damage to the computer's video display.

A third way to provide a video display for 440B-based video boards is to construct and install an ATV Research Pixie Verter on the 440B Board. To accomplish this, you will need to purchase an ATV Research Pixie Verter in kit form, and a 440B Video Board construction manual which outlines the exact details of installing the Pixie Verter. The installation of the Pixie Verter will allow use with an unmodified television set. In any case do not attempt to power up your unit at this time, but simply double check your interconnections and proceed to connecting the keyboard.

G. KEYBOARD INTERCONNECTIONS

The Model 440 Boards are interfaced via a 16-pin socket directly above the phone plug on the video board. The plug accepts a seven-bit input parallel ASCII keyboard with bit 0 being K10 and bit 6 being K16. The plug also has ground present on pin 7, and +5V present on pin 16. An important strobe signal must be provided at pin 9. The keyboard must be a positive, true logic parallel ASCII keyboard. It can have positive, negative continuous, or pulsed strobes. If the unit has a positive going strobe, connect the jumper as shown. If it has a negative going strobe, connect the leftmost donut to the inverted strobe input. These three points are directly between the socket and the phono plug. If you purchase an Ohio Scientific keyboard, it is simply necessary for you to plug the keyboard in at this time. Ohio Scientific also often provides a four-foot interconnecting cable and adaptor PC board called an A-10 kit, which allows you to conveniently fan out the wires from a ribbon cable to a card edge connector or point-to-point wiring. If your video board is equipped with the memory board via three ribbon cables, it is

necessary for you to carefully read and follow the instructions in the special features section for video boards before processing. This is because the graphics option must be inhibited before the computer can be operated. The auxiliary line of ribbon cable connector can be used to provide -9 volts to keyboards which require -9 volts.

There are several keyboards on the market which utilize a General Instruments keyboard encoder chip and require -12 volts. These keyboards will generally not operate on -9 volts and will require an auxiliary power supply, power inverter, or batteries for operation. Once you have connected and checked over your video display interface, and the keyboard interface, you can proceed to actual power-up checkout of your system by going through the section on the 65V PROM Monitor checkout on page 34. Consult the Model 440 Manual for further information.

Part IV-A. 65A PROM MONITOR
(Serial Version)

CHECKOUT. On serial-based systems, once you are confident that you have interfaced the computer correctly, plug in both the terminal and the computer to a common-grounded three-wire outlet. It is also recommended that you not operate the system in areas which produce high static discharges.

First turn on the terminal and allow it to warm up. Then turn on the computer. On systems where you are using your own power supply, monitor the -9V and +5V together with a voltmeter. If the voltage is not 14, turn the power off and check your power supply for malfunctions.

Next, quickly depress the reset switch. On all Challenger systems equipped with BASIC in ROM, the message C/W/M? should be printed out. On systems configured for use with the floppy disk, D/M? should be printed out. On older Challenger configurations, a simple carriage return--linefeed will be put out. Occasionally, on the first reset operation under power-up, one or more of the characters may be mistyped due to warm-up. In any case, repeat the reset procedure several times and observe the output on the screen. If you are not getting the proper message, but are getting a somewhat garbled message of approximately the same length and characters, your baud rate is probably misadjusted. On systems using the 500 Board or on Challenger IIIs (110 baud), it is necessary to fine-adjust the baud rate. A rough adjustment of the baud rate can be made by rocking the potentiometer back and forth over its range and resetting the computer until you get the desired output. If you are not qualified or experienced in electronic servicing, you should not attempt this procedure with power applied. Simply turn the computer off, remove the cover, adjust the potentiometer, place the cover back on, and turn the computer back on (reset) until you get the proper message. If it is not possible to get the proper message with this procedure, check power supply.

Once you have obtained the proper output message, type M. This will place you in the 65A Monitor. Then type P0000. The computer should now start listing memory in columns of eight hexadecimal bytes, or sixteen hex characters with spaces between characters, i.e., 0-9 and A-F, with even spacing between characters. If there are any illegal characters or uneven spaces, then your baud rate requires fine tuning. This can be accomplished by moving the potentiometer baud rate adjustment clockwise until it provides a large number of errors, and then rocking it counterclockwise until it provides a large number

of errors. Then set the potentiometer in the middle of this range.

Proceed now to the 65A PROM Monitor instructions and execute the sample program. If you desire to become familiar with the machine language operation of the computer, refer to the MOS Techonology Programming Manual, which provides an excellent discussion of machine language programming of the computer. Also to Ohio Scientific's Small Systems Journal, which occasionally provides short routines which can be entered directly in machine code. Another excellent introductory source for machine language programming is Ohio Scientific's Model 300 Computer Trainer Manual. This manual provides twenty experiments on the 6502-based Model 300 Computer Trainer, but these experiments can also be executed on any Challenger system. The manual can be ordered directly from Ohio Scientific for ten dollars postpaid.

Once you are satisfied with your familiarity with the 65A Monitor, proceed to Part IV-C, Bringing up BASIC, if your system is so equipped.

INSTRUCTIONS. The 65A PROM Monitor is used with 6502 serial systems by the programmer who wishes to write at the machine language level. When the reset button is pressed, the letters D/M? or C/W/M? appear on the screen. To get into the monitor, type an M on the keyboard (D is used only in conjunction with the diskette, which contains BASIC). While using the Monitor program, you can directly manipulate the computer's memory, and write programs using the computer's own language.

First of all, to examine memory locations before changing them, type a P, then the initial location in the block of addresses you wish to inspect. When you do this, the contents of that block will scroll up the screen. You may halt this scrolling by typing any key on the keyboard.

To change memory contents, type an R to return to the command mode. Then type an L, together with the location whose contents you wish to change, then an optional space for clarity, followed by the "new" contents which you select. If you are altering the contents of consecutive addresses, simply type the new contents one after the other. You may type spaces, carriage returns, and line feeds between these contents if you wish to make it more legible, but this is not necessary. In any case, the next successive address in memory is opened with each set of contents you type. If the next location you wish is not immediately consecutive, type R to get back into the command mode, then type L and the new address, plus the contents you wish to place there. Continue typing new contents if you are changing those of consecutive addresses, otherwise type R, then L, and so on.

To verify any changes you have made, use the P command to examine memory blocks as explained above.

While you are using the L command, the Monitor ignores all non-hexadecimal characters except R. When you use the P command, the Monitor inserts spaces, carriage returns, line feeds, and nulls.

The fourth command available when using the 65A Monitor is the G command, which is used to run programs. This will be illustrated in the sample program below. Some of the following subroutines are used in the course of the program.

Subroutines

```
FE00  INCH (input character and echo)
FE0B  OUTCH (output character)
FE35  CONTROL (Note: FE40 will bypass ACIA initialization)
FE77  LOAD
FE8D  PRINT
```

FEC7 BUILD ADDRESS (constructs an address from input at 00FC [low] and 00FD [high])

Go and Breakpoint Locations

```
0129 Index Register Y
012A Index Register X
012B Accumulator
012C Status Register
012D Stack Pointer
012E Program Counter High
012F Program Counter Low
```

Vectors

```
NMI     0130
RESET   FE35
IRQ     01C0
```

Sample program to illustrate OSI 65A Monitor

This program prints in double any character you type on the keyboard. Beginning at location 0200, the program would look as follows in user-produced source code:

```
10 *=$200
20 JSR INCH
30 JSR OUTCH
40 JM$200
```

The assembled version of this short program would look as follows:

```
10 0200          *=$200
20 0200 2000FE   JSR INCH
30 0203 200BFE   JSR OUTCH
40 0206 4C0002   JMP $200
```

These lines are interpreted as follows:

Line 10: initialization of program counter

Line 20: actual program begins at given initialization point (0200); 20 is the ASCII code representation for JSR; 00 is the low address byte of INCH; FE is its corresponding high address byte.

Line 30: since three bytes have been used since program initialization, we are now at location 0203; 20 is ASCII for JSR; 0B is low address byte for OUTCH; FE is its corresponding high address byte.

Line 40: as this is the sixth byte since program initialization, we are at location 0206; 4C is the ASCII code for JMP; 00 is the low address byte for location 0200; 02 is its corresponding high address byte.

The bytes in this program are all to occupy consecutive memory locations. Therefore, only one L command will be necessary while we are in the Monitor, until we are ready to run the program. To enter it, type an M in response to D/M?, and then type an L. Following this, type each byte in the program in consecutive order, i.e., 02002000FE200BFE4C0002. Finally type R to get back into the command mode.

To verify that these contents are loaded into memory, type P0200. The contents of all the addresses beginning with location 0200 (i.e., the program which you have just entered) will immediately scroll up

the screen. When all the contents you wish to see have appeared, type R to get back into the command mode.

To run the program, you need to set the stack pointer (located at address 012D to 28, and the program counter high (012E) at 02 and low (012F) at 00, because the starting address is 0200. Since these locations are consecutive, you need only type: L012D280200R. To execute the program, type G. Then any character you type will appear in duplicate on the screen.

Part IV-B. 65V PROM MONITOR
(Video Version)

CHECKOUT. Once you have carefully checked out the interfacing between your video monitor and, optionally, your keyboard, connect the monitor and computer to a common grounded three-wire outlet in an area not susceptible to static discharges. Turn the monitor on and readjust it for a dark screen with mid-range contrast. Then momentarily turn the computer on. You should see a random field of alphabetic and numeric characters. Occasionally the computer will automatically reset on power-up, causing the screen to go blank and display only a few characters. Turn the computer on and off a few times to assure a non-reset condition, or random field of characters. It will now probably be necessary to adjust horizontal and vertical hold to get a stable display of these characters. If you cannot obtain these result, check your power supply.

On systems utilizing the 440B Video Board, it will probably be necessary for you to adjust your video display for underscanning to get at least 24 lines of 24 characters on the screen, the recommended minimum for use with Ohio Scientific software. The height of the television display can usually be changed by simply adjusting the vertical control. Some sets have horizontal control. Other sets will require reduction in the power supply voltage by simply turning down the power supply adjustment. The centering rings on the back of the monitor's picture tube can then be adjusted to your liking. Once the video display has been set up at least to the point of legibility, depress the reset switch momentarily and release it. On all systems with BASIC in ROM, the message C/W/M? should appear in the lower left corner of the screen. On systems configured for disk, the message D/M? should appear in the lower left corner of the screen. On systems with neither of these features, four zeros followed by a space and two random hexadecimal digits should appear in the upper left corner of the screen. If the screen clears, but only part of the display just described is present, it is possible that you have not underscanned the set adequately, or it may be necessary for you to adjust the vertical and horizontal controls to bring this portion of the display onto the screen. Once you have obtained this message on the screen, type an M on the keyboard to get into the Monitor command mode. At this time you should see four zeros followed by a space and two random hexadecimal digits in the upper left portion of the screen.

Now, following the instructions for the OS-65V PROM Monitor, you should be able to change data and enter the short demonstration program on your system.

If you wish to become more familiar with the machine language programming for your system, refer to the MOS Technology 6502 Programming Manual, Ohio Scientific's Small Systems Journal, and Ohio Scientific's Model 300 Computer Trainer Manual, which provides twenty experiments for self-taught machine code on any 6502 system. The manual is directly available from Ohio Scientific for ten dollars

postpaid.

Once you have become familiar with the operation of the 65V PROM Monitor, proceed to Part IV-C.

INSTRUCTIONS. Anyone wishing to become proficient in programming at the machine language level should be well acquainted with the PROM Monitor, which is necessary to examine and change the contents of memory locations. The Monitor used in conjunction with the 6502 video system is the OSI 65V PROM Monitor.

If BASIC ROMs are present in your system, OSI's 8K BASIC comes up when the computer is reset. When this is done, the letters C/W/M? or D/M? (the latter on systems configured for disk operation) appear on the video screen or terminal. If you wish to enter a program by means of the monitor instead of in BASIC, type an M on the keyboard. If BASIC ROMs are not present, the computer always comes up in the Monitor. Whichever way the Monitor is brought in, it always starts in the address mode, that is, the mode in which you can specify memory addresses or locations and examine their contents. Appearing on the screen are four digits in hexadecimal notation followed by two and, finally, another two digit number, also in hex. The four-digit number is a location, and the two digits are the contents of that location. To examine another address, type the address on the keyboard. The same address will appear on the terminal, as will the corresponding contents of that address.

If you wish to change those contents and thus enter programs using the Monitor, you must exit the address mode and get into the data mode. To do this, type a slash (/). Then type any two hex characters, which will be inserted into that location as its new contents. The normal procedure for entering programs via the Monitor is to use consecutive memory locations. While still in the data mode, you can open the next address by typing the return key. You can do this continually, each time altering the memory contents according to the needs of the program you are writing. If you want to jump to a non-consecutive location, you need to get back into the address mode by typing a period. Then type the new address you want. Type another slash to get back into the data mode and continue as before until you want to open another non-consecutive address. Use extreme caution whenever the Monitor is in the data mode, as you are directly manipulating the computer's memory.

If you wish to enter a program from an audio cassette instead of manually from the keyboard, first get into the address mode (type a period), then turn on the cassette. Let the tape advance to the point where the program of interest begins, and type L. This transfers control to the audio cassette, such that all ASCII commands are supplied by the cassette instead of by the keyboard. The L command also puts the Monitor into the data mode. If the contents of 00FB are 00, the Monitor will accept commands from the keyboard.

If the cassette does not load 00FB (hex) with 00, press reset to transfer control back to the keyboard. Otherwise, commands are accepted from the audio cassette UART.

To run any program which you have entered via the Monitor, get into the address mode, type the starting address of the program, and type a G.

Label	Program Entry Points
VM	FE00 - Restart Location

FE0C - Bypasses UART and Stack Pointer initialization and the clearing of decimal mode, but does not clear the screen.

IN FE43 - Entry into address mode, bypass initialization

INNER FE77 - Entry into data mode, bypass initialization

Label Subroutines

OTHER FE80 - Input an ASCII character from audio cassette UART

LEGAL FE93 - Returns stripped ASCII number if 0-9 or A-F. Otherwise returns an FF.

INPUT FEED - Input an ASCII character from keyboard.

Required Hardware

The 65V Monitor requires as a minimum the following hardware: an OSI Model 400 Board with a 6502 microprocessor, 1,024 words of RAM memory located from 0000 to 03FF, and the 65V monitor itself. It also requires an OSI Model 440 Board populated for alphabetic display and keyboard input. The 440 Video Board must be located at DXXX, which will automatically located the keyboard input at DFXX.

The keyboard must be a seven-bit high true ASCII keyboard with a positive or negative going strobe pulse at least 100 microseconds long.

The 65V Monitor will additionally support input from a generalized serial communications subsystem of an OSI 430 Board-based audio cassette interface. The same program can be used with a 430 Board configured for digital cassette or ASCII teletype input.

Commands:

Address Mode Commands:

/ - change to data mode.

G - Go -- Jump to location seen on screen and execute program found there.

L - Transfer control to audio cassette.

Data Mode Commands:

. - Change to address mode

<return> - open next address, i.e., increment location counter by 1.

If the 65V is in address mode, typing 0 to 9 or A to F will cause that number to be rotated into the least significant digit (LSD) of the location pointer. Typing a 4, for example, causes 0123 XX to become 1234 XX.

If it is in the data mode, the number is rotated into the data contents and memory is thus modified. This permits the easy correction of errors. If, for instance, the user typed 0478 when intending to look at location 047B, he would simply type 047B.

All of the non-command keys and non-hexadecimal characters are ignored by the monitor.

Demonstration Program:

The following is a program which may be entered by use of the 65V Monitor from the keyboard or audio cassette. A * indicates a return key depression.

.0002 Loads the ASCII Message starting at location 0002.
4F*53*49*20*36*35*56*2E*5F

.0200 Loads the Main Program a 0200
/A9*02*A2*00*20*00*03*A2*00*20*ED*FE*9D*24*D2*E8*4C*09*02

.0300 Loads the Subroutine at 0300 to output an ASCII character string.
/85*00*A9*00*85*01*A0*00*B1*00*C9*5F*F0*0A*9D*E4*D1*E8*E6*00*D0*F2*E6*01*60

.0200G Loads the starting address of the program and executes it. You should see the message OSI 65V. appear on the screen. Now you may type any keys and they will be echoed just below the message. Press reset to reenter the 65V Monitor.
If this were entered off of the audio cassette, it would be self-loading and auto starting. Since the cassette is in complete control, it can load the starting address and execute the program without user interruption.

Part IV-C. BRINGING UP BASIC

Once you have dabbled a little with machine language programming, you will be eager to get on with full BASIC. If your machine is equipped with BASIC in ROM, it will not be necessary to connect any additional devices to get to BASIC. Simply reset the computer and type C in response to C/W/M? The computer then asks MEMORY SIZE? Reply with a carriage return. The machine then asks TERMINAL WIDTH? to which you may also reply with a carriage return. The BASIC prompter OK will then come up, indicating that BASIC is directly accessible. You may then wish to connect an audio cassette interface, if one is present in your system.

If your computer is configured for floppy disk, it will be necessary to connect a disk drive before you can bring BASIC in. The computer must have at least 16K RAM, floppy disk bootstrap PROM (indicated by the message D/M? when the computer is reset), and a 475 floppy disk controller board present in the computer. When the floppy disk controller board is present, it is usually the rearmost board in the computer system. With the computer turned off, connect the ribbon cable coming out of the rear of the floppy disk drive in one of the openings in the rear of the Challenger and mate it with one of the connectors coming out of the back of the 470 Board. This should be accomplished such that the ribbon cable falls into the case instead of sticking up out of it. The boards should be mated tightly together and the connector should be backed off about 1/8" to preclude the possibility of the Molex pins touching the PC board foils on the A-12 adaptor board of the cable. That is, you should be sure that the Molex pins on the 470 Board are not touching the A-12 adaptor cable board. Then make sure that all parts of the computer are plugged into a common grounded three-wire outlet or distributor box on one circuit. Power up the floppy disk drive. Place a diskette with OS-65D in the disk drive (the upper drive on dual disk drives) with the label side up and the notched edge in first. Follow the dialog and procedures on pages 1 to 4 of the OS-65D Version 2.0 Manual. After you have obtained the BASIC prompter OK, proceed with the example in this manual, if desired.

If your system is equipped with neither the floppy disk nor BASIC in ROM, you must load BASIC via paper tape or audio cassette. You

must have at least 12K of memory to do so. Paper tape versions of BASIC are specifically designed for use with Teletypes while the audio cassette version is for use strictly with video-based computer systems. Follow the instructions at the end of the 8K BASIC User's Manual on paper tape. Follow the instructions included here on the use of Auto-Load audio cassettes, and then proceed to the end of the 8K BASIC User's Manual for instructions on loading 8K BASIC audio cassettes. This procedure is necessary only if you do not have BASIC in ROM or on disk.

All of the special features of Ohio Scientific's 6502 8K BASIC are described in the OSI 8K BASIC User's Manual. For a more fundamental introduction into BASIC, refer to any of the following books:

Gottfried, B. S., Programming with BASIC, Schaum's Outline Series, McGraw-Hill, New York, 1975.

Gottfried, B. S., BASIC Programmer's Reference Guide, Quantum Publishers, New York, 1973.

Greunberger, F., Computing with the BASIC Language, Canfield Press, San Francisco, 1969.

Kemeny, J. G., and T. E. Kurtz, BASIC Programming, 2nd ed., Wiley, New York, 1971.

Part IV-D. AUDIO CASSETTE

The Challenger system offers an audio cassette interface based on the popular 430B I/O Board. The interface uses the popular and ultra-reliable Kansas City Standard for Audio Cassette information storage technique. The interface requires the use of a medium quality audio cassette recorder such as the Panasonic RQ-309 and medium to high-quality audio cassettes. We recommend that you not use audio cassettes longer than C-30s. In this way you will minimize drag and speed variations. The connections between the recorder and the interface are simply interface output, microphone input, and interface input from cassette speaker output. These cables should be fabricated from standard shielded microphone cable.

On systems with a 430B I/O Board, it will be necessary to connect to a male Molex connector which mates with the 430B Board's output connectors. Consult the Model 430B Manual for connector pinouts. The audio cassette interface is supported by the 65V PROM Monitor, BASIC in ROM, and OS-65D Disk Operating System. All three of these have cassette I/O capability.

The most popular use of the audio cassette interface is as program and data storage for BASIC in ROM computers. The audio cassette interface can be used with any Ohio Scientific BASIC in ROM computer which is configured either for video display or for serial output with a baud rate above 300. The procedure for using the audio cassette interface in conjunction with an audio cassette to store a program in BASIC is as follows:

First, complete the program to your satisfaction in the BASIC's editor workspace.

Second, connect the the audio cassette recorder, turn it on, and place an erased or blank cassette in the unit.

Third, type SAVE, <carriage return>, and LIST, without carriage return. Turn the tape recorder on record with volume and tone set mid-range. Allow the tape to advance past the white leader. As soon

as the recording tape is on the take-up reel, type <carriage return>. The program will then list out both the screen and the cassette recorder at 300 baud. When the listing is complete, turn off the tape recorder and type LOAD, <carriage return>, and <carriage return>. This will turn off the cassette output and return the display to full speed. To play a new program back into the BASIC workspace, reset the computer or type NEW <carriage return>. This will empty the computer's workspace. Then type LOAD, turn the cassette recorder on play, and as soon as the tape advances past the white leader, type <carriage return>.

As soon as the cassette encounters the program on the tape, it should start listing on the screen as it goes through the cassette. Be careful not to type any key after you type <carriage return> following LOAD, since that would automatically bring the machine out of cassette load. Typing any key is the way to exit cassette loading mode. Once the program is complete, the program should be played back into the machine flawlessly and at the very end, the tape will put out an OK. OK will cause the BASIC interpreter in the machine to report a syntax (SN) error. This is the normal operation of the computer. Once the loading is complete, simply type any key on the keyboard (e.g., an additional <carriage return>) to exit the cassette loading mode. Then turn the cassette recorder off.

WHAT'S NEXT? Ohio Scientific's powerful 8K BASIC opens up broad areas for your investigation of both pre-written programs and the opportunity to write your own original programs for entertainment, education, and possibly your own business applications. Programs and programming techniques for BASIC, along with many applications ideas, can be found in Ohio Scientific's Small Systems Journal, and the small computer magazines such as BYTE, Interface Age, and Kilobaud. The system also has full capabilities for machine language programming, such as an Assembler, and directly in machine code. Again, Ohio Scientific's Small Systems Journal and several of our pre-packaged programs provide an excellent insight into this area. Several Ohio Scientific dealers and representatives are also providing full applications program packages for small businesses and for industrial users for use in conjunction mainly with eight-slot disk-based Ohio Scientific computer systems. Read Ohio Scientific's Small Systems Journal for details on software for the computer systems. We would also welcome your contribution to the Journal as a user. The Journal is both a user's group forum and a factory forum. See subscription information at the front of this manual.

Part V.

APPENDICES

I. Parts Lists
II. Errata
III. Logic Probe
IV. Table of Enables
V. I/O Connectors
   Interface Connections
   TTY Connections
VI. Power and Ground
   Ohio Scientific Bus Pinout
VII. System Expansion

PARTS LIST FOR 504A KIT

	Quantity	Part	Location
Integrated Circuits	1	74Ø0	B5
	5	74Ø4	C5 C6 F2 F9 F11
	4	7417	C1 C2 C3 F1
	4	742Ø	B3 B4 F3 F5
	1	743Ø	F6
	1	74123	B2
	4	8T26	B8 B9 C9 C1Ø
	1	555	C4
	1	65Ø2	A2
	1	685Ø	A3
	1	65A-Monitor (17Ø2 PROM)	A5
	8	21Ø2	D1-D8

Appendix I.

Resistors

R1 - 39Ø	R11 - 4.7K	R19 - 1ØØ
R2 - 22Ø	R12 - 1K	R22 - 4.7K
R3 - 4.7K	R13 - 47Ø	R23 - 1K
R4 - 4.7K	R14 - 47Ø	R24 - 1K
R6 - 4.7K	R15 - 47Ø	R34 thru R49
R7 - 4.7K	R16 - 39Ø	- 47Ø (16 Resistors)
R8 - 4.7K	R17 - 1K	R5Ø - 1ØK Trimpot
R1Ø - 22K	R18 - 22K	R51 - 5K Trimpot

Total Resistor Count:

Value	Count
1ØØ	1
22Ø	1
39Ø	2
47Ø	19
1K	4
4.7K	7
22K	2
10K Trimpot	1
5K Trimpot	1

Capacitors

C2 - 82pf
C3 - 82pf
C4 - .01uf
C5 - .01uf Mylar
C11 - .1uf

15 - .1uf Bypass Capacitors

Diodes

D1 - 1N914
D2 - 1N914
D3 - 1N914
D9 - 1N914

PARTS LIST FOR 504V KIT

	Quantity	Part	Location
Integrated Circuits	1	74ØØ	B5
	4	74Ø4	C6 F2 F9 F11
	4	7417	C1 C2 C3 F1
	3	742Ø	B4 F3 F5
	1	743Ø	F6
	1	74123	B2
	4	8T26	B8 B9 C9 C1Ø
	1	65Ø2	A2
	1	65V-Monitor (17Ø2 PROM)	A5
	8	21Ø2	D1-D8

Appendix I.

Resistors

R3 - 4.7K
R4 - 4.7K
R6 - 4.7K
R7 - 4.7K
R8 - 4.7K
RlØ - 22K
Rll - 4.7K
Rl2 - 1K
Rl3 - 47Ø
Rl4 - 47Ø
Rl5 - 47Ø
Rl7 - 1K
Rl8 - 22K
R34 thru R49
- 47Ø (16 Resistors)
R5Ø - 1ØK Trimpot

Total Resistor Count:

Value	Count
47Ø	19
1K	2
4.7K	6
22K	2
10K Trimpot	1

Capacitors

C2 - 82pf
C3 - 82pf

15 - .luf Bypass Capacitors

Diodes

Dl - 1N914
D2 - 1N914
D3 - 1N914
D9 - 1N914

COMPREHENSIVE PARTS LIST FOR MODEL 500

	Quantity	Part	Location	
Integrated Circuits	1	74ØØ	B5	
	5	74Ø4	C5 C6 F2 F9 F11	
	4	7417	C1 C2 C3 F1	
	9	742Ø	B3 B4 C7 C8 F3 F4 F5 F8 F1Ø	
	2	743Ø	F6 F7	
	1	74123	B2	
	1	555	C4	
	4	8T26	B8 B9 C9 C1Ø	
	1	6502	A2	
	1	682Ø	A1	
	1	685Ø	A3	
	3	17Ø2A	A4 A5 A6	Monitor PROMs
	4	ROM	A7 A8 A9 A10	BASIC ROMs
	32	21Ø2	D1 - D8 (ØK) D1 - E8 (1K) D9 - D16 (2K) E9 - E16 (3K)	

Resistors

R1 - 39Ø
R2 - 22Ø
R3 - 4.7K
R4 - 4.7K
R5 - (omitted)
R6 - 4.7K
R7 - 4.7K
R8 - 4.7K
R9 - 4.7K
R1Ø - 22K
R11 - 4.7K
R12 - 1K
R13 - 47Ø
R14 - 47Ø
R15 - 47Ø
R16 - 39Ø
R17 - 1K
R18 - 22K
R19 - 1ØØ
R2Ø - 47Ø
R21 - 47Ø
R22 - 4.7K
R23 - 1K
R24 - 1K
R25 - 1ØK
R26 - 4.7K
R27 - 47Ø
R28 - 1ØK
R29 - 1ØK
R3Ø - 1K
R31 - 43Ø
R32 - 1Ø
R33 - 47Ø
R34 thru R49 - 47Ø
R5Ø - 1ØK Trimpot
R51 - 5K Trimpot

Total Resistor Count:

Value	Count
1Ø	1
1ØØ	1
22Ø	1
39Ø	2
43Ø	1
47Ø	23
1K	5
4.7K	9
1ØK	3
22K	2
5K Trimpot	1
1ØK Trimpot	1

Capacitors

C1 - 25uf 10v
C2 - 82pf
C3 - 82pf
C4 - .01uf
C5 -
C6 -
C7 -
C8 -
C9 -
} Baud Rate Capacitors (Value Depends on Desired Baud Rate)
C1Ø - .1uf
C11 - .1uf

Diodes

D1 -
D2 - } 2-Speed Clock Option
D3 - DD (PROM)
D4 - Serial Interface
D5 -
D6 - } WAIT (ROM)
D7 - DD (ROM)
D8 - WAIT (PROM)
D9 - DD (RAM)
D1Ø - WAIT (RAM)
D11 - WAIT (PIA)

Transistors

Q1 - 2N5225 or equal
Q2 - 2N5226 or equal
Q3 - 2N398 or equal

All Diodes-1N914

Resistors

R1 - 39Ø
R2 - 22Ø
R3 - 4.7K
R4 - 4.7K
R5 - (omitted)
R6 - 4.7K
R7 - 4.7K
R8 - 4.7K
R9 - 4.7K
R1Ø - 22K
R11 - 4.7K
R12 - 1K
R13 - 47Ø
R14 - 47Ø
R15 - 47Ø
R16 - 39Ø
R17 - 1K
R18 - 22K
R19 - 1ØØ
R2Ø - 47Ø
R21 - 47Ø
R22 - 4.7K
R23 - 1K
R24 - 1K
R25 - 1ØK
R26 - 4.7K
R27 - 47Ø
R28 - 1ØK
R29 - 1ØK
R3Ø - 1K
R31 - 43Ø
R32 - 1Ø
R33 - 47Ø
R34 thru R49 - 47Ø
R5Ø - 1ØK Trimpot
R51 - 5K Trimpot

Total Resistor Count:

Value	Count
1Ø	1
1ØØ	1
22Ø	1
39Ø	2
43Ø	1
47Ø	23
1K	5
4.7K	9
1ØK	3
22K	2
5K Trimpot	1
1ØK Trimpot	1

Capacitors

C1 - 25uf 10v
C2 - 82pf
C3 - 82pf
C4 - .01uf
C5 -
C6 -
C7 -
C8 -
C9 -
} Baud Rate Capacitors (Value Depends on Desired Baud Rate)
C1Ø - .1uf
C11 - .1uf

Diodes

D1 -
D2 - } 2-Speed Clock Option
D3 - DD (PROM)
D4 - Serial Interface
D5 -
D6 - } WAIT (ROM)
D7 - DD (ROM)
D8 - WAIT (PROM)
D9 - DD (RAM)
D1Ø - WAIT (RAM)
D11 - WAIT (PIA)

Transistors

Q1 - 2N5225 or equal
Q2 - 2N5226 or equal
Q3 - 2N398 or equal

All Diodes-1N914

Appendix II

Errata

The following corrections must be made to all Rev. A series Model 500 Boards (these have no revision letter near the board label):

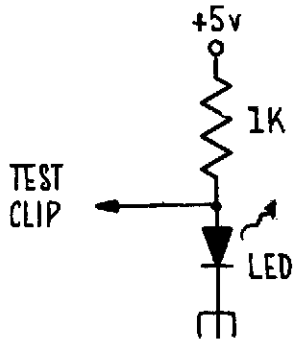
1. Cut the foil which runs from IC-D10 p. 14 on top of the board. Locate the small donut on the front of the board immediately to the right of IC-B2 p. 15 (this donut connects with IC-B3 p. 12 on the rear of the board). Locate the small donut below IC-A1 p. 21 (this donut connects with IC-A1 p. 21 on the front of the board). Install a jumper between these two donuts.

2. Locate the two small donuts immediately to the left of backplane connectors B13 and B14. The top donut connects to IC-B7 p. 5. The bottom donut connects to backplane connector B43. Install a short jumper between these two donuts.

3. (For RS-232 option) Do not install R28 in the location marked on the overlay. Instead, install it at location marked R31. Locate the oval pad below R31 (this connects with the bottom donut of R31 on the front of the board). Locate the top donut of location R28 (this donut connects to the collector of Q2 on the rear of the board). Install a jumper between these two donuts.

Appendix III.

Logic Probe



This simple logic probe will indicate the state of a TTL output under static conditions. It will also operate under dynamic conditions if the signal is being strobed at a high rate, however, it will not "catch" a pulse or indicate a low-duty-cycle signal.

To operate, connect to system power and ground where shown. Connect the test clip to the circuit point under test. The LED will

TABLE OF ENABLES

Enable	Function	Source Pin	Destination Pin	Active Level	Diagram
0000·(02·VMA) -03FF·(02·VMA)	2102	IC-F3 p. 8	Bank 0 p. 13	lo	3
0400·(02·VMA) -07FF·(02·VMA)	RAM	IC-F4 p. 6	Bank 1 p. 13	lo	3
0800·(02·VMA) -08FF·(02·VMA)	ENABLE	IC-F4 p. 8	Bank 2 p. 13	lo	3
0CXX (02 VMA) -0FFF·(02·VMA)		IC-F5 p. 6	Bank 3 p. 13	lo	3
0XXX·R/W·(02·VMA)	RAM	IC-F11 p. 8	IC-B8 p. 1,15	hi	3
	8T26 ENABLE		IC-C9 p. 1,15	hi	3
FCXX·(02·VMA)·R/W	ACIA	IC-B3 p. 6	IC-A3 p. 9	lo	4,7
FDXX·(02·VMA)·R/W	PROM	IC-B3 p. 8	IC-A4 p. 14	lo	4
FEXX·(02·VMA)·R/W	PROM	IC-B4 p. 6	IC-B5 p. 4	lo	4
FFXX·(02·VMA)·R/W	PROM	IC-B4 p. 8	IC-B5 p. 5	lo	4
R/W·(02·VMA)· (FEXX+FFXX)	PROM	IC-B5 p. 8	IC-A5 p. 14	lo	4
A000·(02·VMA)·R/W -A7FF·(02·VMA)·R/W	ROM	IC-C6 p. 2	IC-A7 p. 20	hi	5
A800·(02·VMA)·R/W -AFFF·(02·VMA)·R/W	ROM	IC-C6 p. 10	IC-A8 p. 20	hi	5
B000·(02·VMA)·R/W -B7FF·(02·VMA)·R/W	ROM	IC-C6 p. 8	IC-A9 p. 20	hi	5
B800·(02·VMA)·R/W -BFFF·(02·VMA)·R/W	ROM	IC-C6 p. 4	IC-A10 p. 20	hi	5
F7XX	PIA	IC-F7 p. 8	IC-A1 p. 23	lo	8

Explanation:

ENABLE shows the logical composition of the enable signal. When testing, set up the address shown. 02·VMA (p. 39 of the microprocessor, labeled "02") and R/W will normally drift high.

Source pin and destination pin(s) show the pin where the signal originates and the chip(s) being enabled, respectively.

Active level indicates a hi-true or a low-true enable.

(UPPER LEFT CORNER OF BOARD.
VIEW FROM FRONT.)

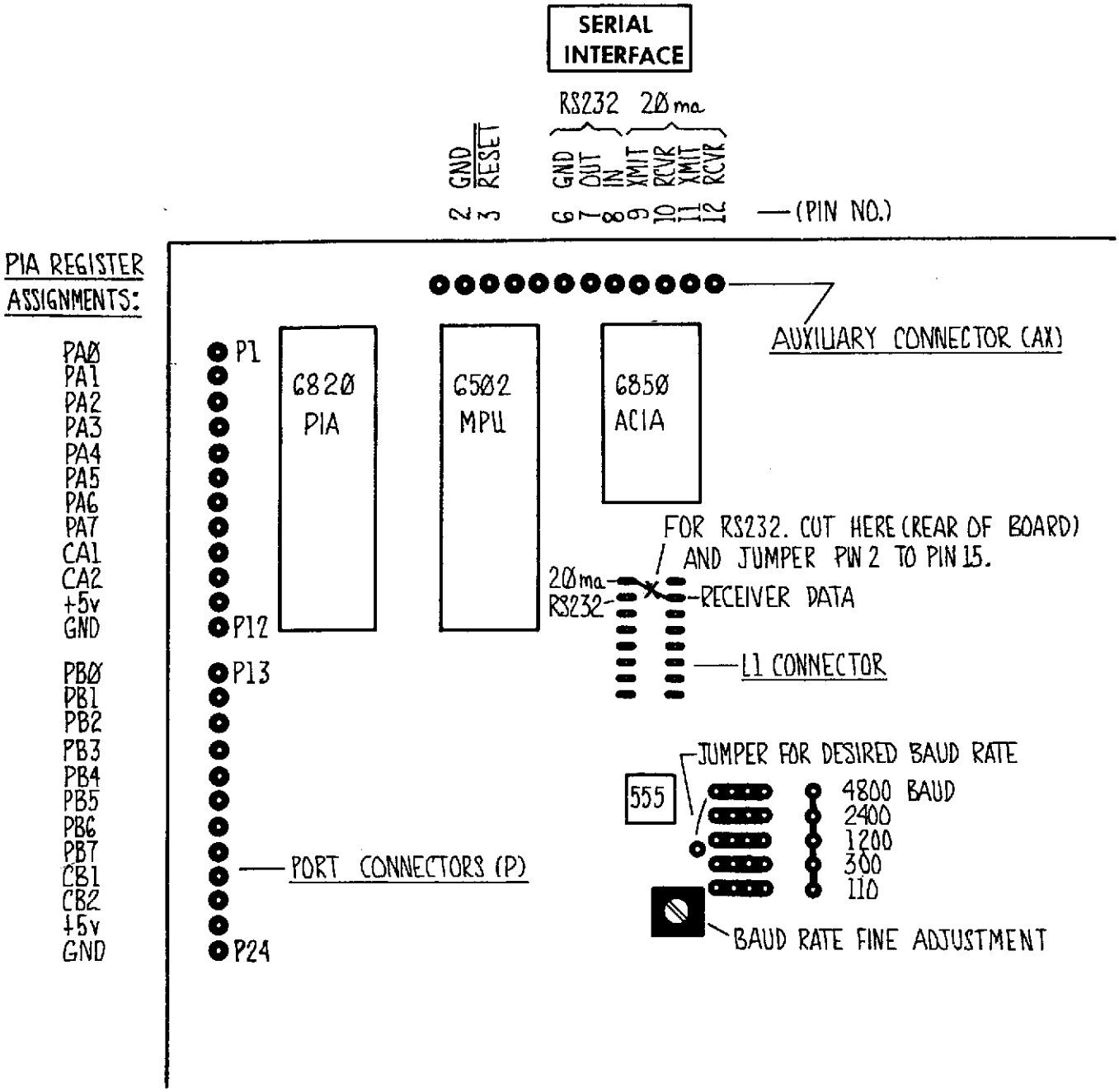


TABLE OF BAUD RATE CAPACITOR VALUES

	MIN	MID-RANGE	MAX
4800 BAUD	.001 µf	.002 µf	.0027 µf
2400	.0022	.0033	.0056
1200	.0045	.0068	.0110
300	.0179	.027	.0446
110	.0489	.082	.1216

MID-RANGE CAPACITANCE VALUES ARE RECOMMENDED, HOWEVER ANY VALUE BETWEEN MIN AND MAX MAY BE SUBSTITUTED. ALL VALUES ARE IN µf.

MODEL 500 I/O CONNECTIONS

Appendix V.

TABLE ONE

INTERFACE CONNECTIONS

500, 510 Auxiliary Connector	Description	EIA Standard Pinout
6	RS-232 Ground	7
7	RS-232 output from CPU (input to terminal)	3
8	RS-232 input to CPU (output from terminal)	2
9	20ma loop CPU output (+) connect to pin 7 on TTY	13
10	20ma loop CPU input (+) connect to pin 4 on TTY	12
11	20ma loop CPU output (-) connect to pin 6 on TTY	25
12	20ma loop CPU input (-) connect to pin 3 on TTY	24

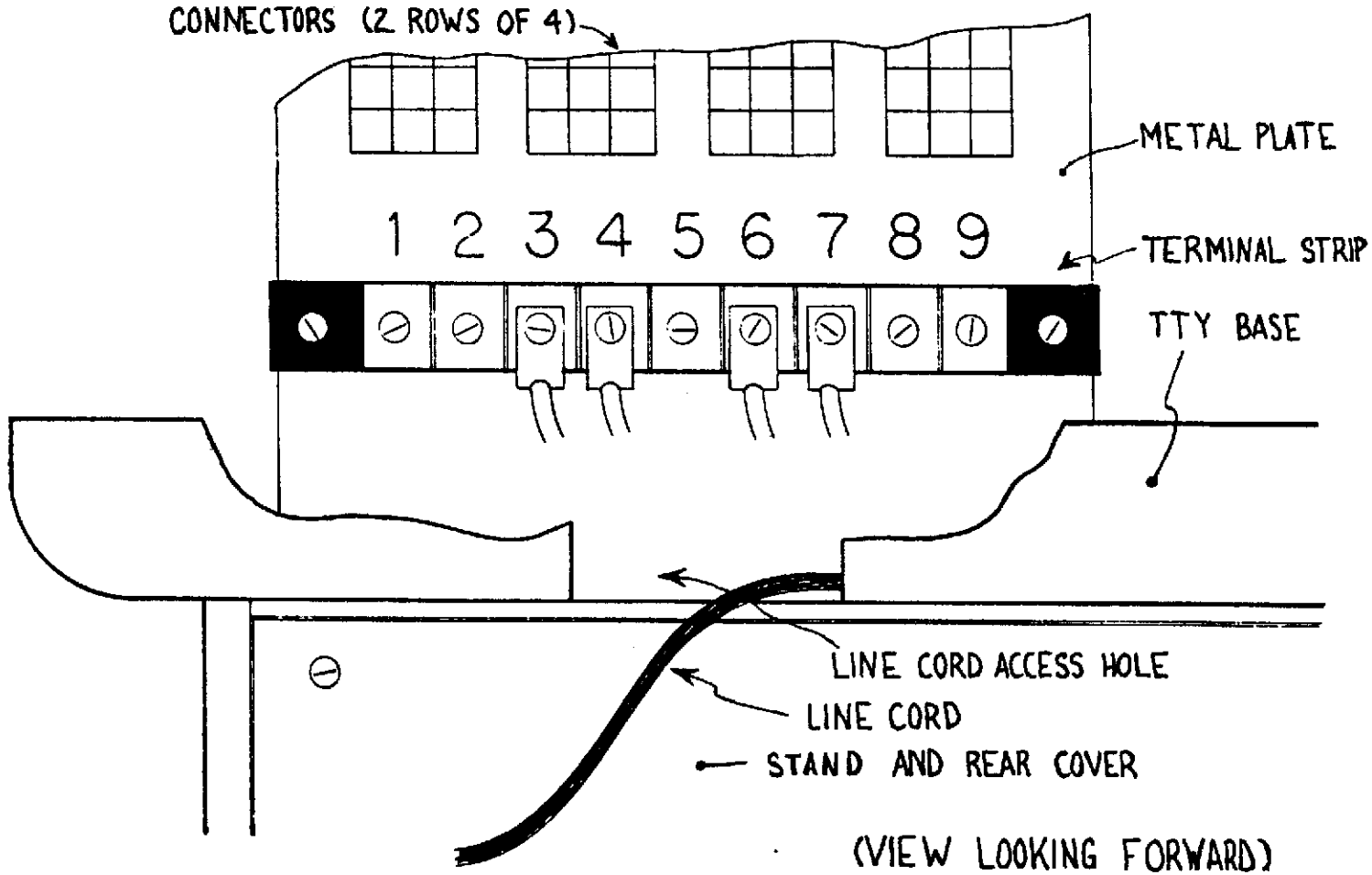
TABLE TWO

PIN CORRESPONDENCE CHART FOR A-10 CABLE

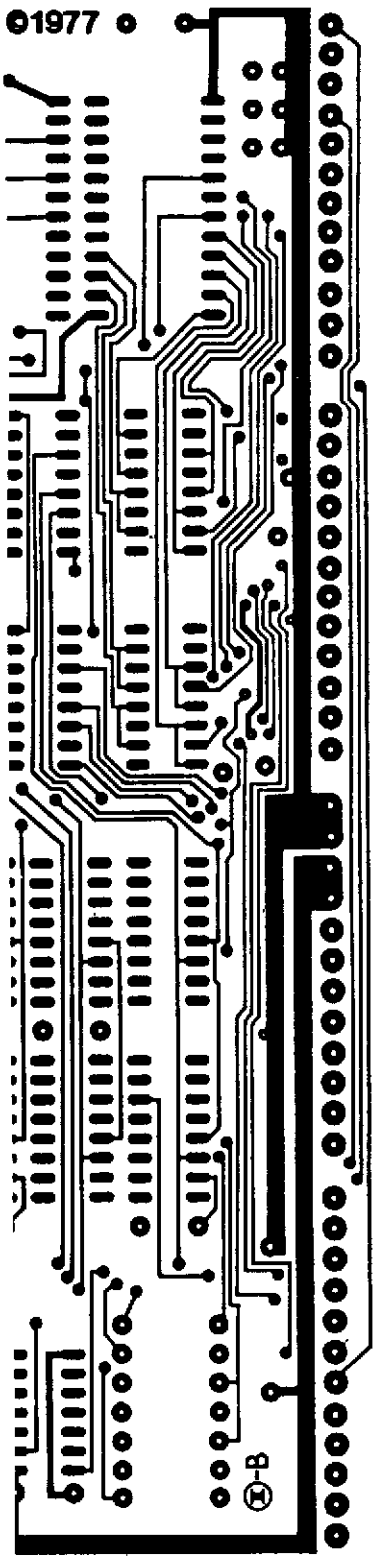
Molex Pin #	IC PIN #
M1	C16
M2	C1
M3	C2
M4	C3
M5	C4
M6	C5
M7	C6
M8	C7
M9	C9
M10	C10
M11	C11
M12	C8

Note: C12, C13, C14, and C15 may optionally be jumpered to any M-Pin by cutting foil as shown.

Appendix V.



Connecting to a Teletype



(THIS IS TOP RIGHT FRONT CORNER OF THE BOARD.)

B24- -9v @500 ma.

B25, B26- +5v @2A

B27, B28- GND

NOTE: POWER SUPPLY CURRENT REQUIREMENTS ARE FOR FULLY POPULATED BOARD.

MODEL 500 - POWER CONNECTIONS

Appendix VI.

BACKPLANE CONNECTORS:

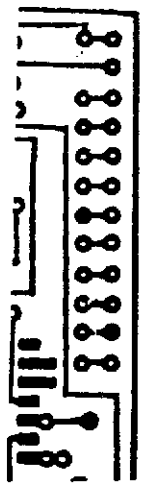
B1 - WAIT
2 - $\overline{\text{NMI}}$
3 - $\overline{\text{IRQ}}$
4 - Data Direction
5 - D0
6 - D1
7 - D2
8 - D3
9 - D4
10 - D5
11 - D6
12 - D7

B13 - D8
14 - D9
15 - D10
16 - D11
17 - $\overline{\text{Reset}}$
18 ---------
19 - A19
20 - A18
21 - A16
22 - A17
23 - +12volts
24 - -9volts

B25 - +5volts
26 - +5volts
27 - ground
28 - ground
29 - A6
30 - A7
31 - A5
32 - A8
33 - A9
34 - A1
35 - A2
36 - A3

B37 - A4
38 - A0
39 - Ø2
40 - R/W
41 - VMA
42 - Ø2·VMA
43 - A10
44 - A11
45 - A12
46 - A13
47 - A14
48 - A15

AUXILIARY CONNECTOR:



AX1 - Processor RDY or $\overline{\text{HLT}}$
2 - Power Ground
3 - $\overline{\text{Reset}}$
4 - (Unused)
5 - (Unused)
6 -
7 - Ground
8 - Output } RS232C
9 - Input
10- Serial Receiver
11- Serial Transmitter
AX12- Serial Receiver Gor -

Appendix VII.

SYSTEM EXPANSION

This very important App Note covers the recommended OSI 500 expansion configuration and acts as the manual for the OSI Model 480 Backplane Board.

The memory maps on the following page specifies systems directly supported by OSI software, that is, software which is or will be available to run on these systems without modification. The Model 480 Backplane Board is designed to connect together eight 400 or 500 series boards in a single processor system.

A. System with two to eight slots

Refer to the attached 480 diagram. The 480 Backplane rear surface is the side with conductive foil. This discussion is for operation with two to eight slots. Eight to thirty-two KK-156 series Molex connectors are inserted through the front of the board and soldered in place as indicated by the thirty-two black lines. Power connections can be made via the right card edge or an unused slot with wires or KK-156 connectors. If the right edge is used, a jumper should be placed on B24 across the prototyping area labeled E. If two or three slots are being used, this is all that needs to be done. Any board can be placed in any slot on the board (1 through 8 inclusive) so long as only one is a CPU board and no two boards have the same memory address.

The CPU board should be located at slot 8 for the cleanest bus signals, and the 440 Video Graphics Board should be located at slot 1 to minimize video pickup of logic noise.

Summary of two to eight-slot use:

1. Install eight to thirty-two Molex connectors.
2. Connect ground +5, -9, and and any other supply voltages.

B. System with nine or more slots

The 480 Boards may be linked together to provide up to 250 slots via the following procedure. After eight slots are used, the twenty address and control lines from the processor (B29 to B48) must be buffered every eight slots via 7417s to drive the next eight slots. Similarly the four open collector or wired control lines B1 to B4 to the processor must be buffered every eight slots via 7417s. Since the 7417s are symmetrical, they can be rotated 180 degrees on the board to define the signal direction on the board. The recommended configuration is to add additional backplanes to the right. That is, slot 8 of the main motherboard would be closest to slot 1 of the first expansion board.

For this configuration, the four 7417s on the main motherboard would be installed such that pin 14 of each 7417 is at (B). Pin 14 of each 7417 (B) would be connected to the +5 bus and pin 7 of each 7417 (A) would be connected to ground. If only one expansion board is used, the expansion board will not need 7417s. If three or more backplanes are used, all but the last board will require buffers. Each expansion backplane board will require the twenty 220-ohm pullups indicated by H and will additionally require the 4.7K pullups at B1 to B4 as indicated by G. The backplane boards may be connected together via wire jumpers (be sure to connect +5 only to B25 and B26) or via KK-156 series Molex connectors. The standard right angle female Molex connectors can be installed at the right side of

the board by shearing off about 1/4" of the board (indicated by C). The holes at the end of the board are large enough to accept both the connectors and the pullup resistors. However the resistors will have to be stood up on end with a lead going to +5. Standard male Molex connectors can be used on the mating board by bending the pins to a right angle with pliers, or, preferably, right angle Molex connectors can be used.

Summary of board instructions with nine or more slots:

1. Follow steps 1 and 2 of instructions for two to eight slots.
2. Install four 7417s as indicated in the diagram with pin 14 corresponding to (B).
3. Jumper pin 14 (B) of each 7417 to +5 and pin 7 (A) to ground.
4. On each accessory board, follow step 1, above. Install the pullup resistors at the same time as the interconnection jumpers or connectors. Include the four 4.7K pullups indicated by G on the diagram.
5. On all but the last accessory board, follow steps 2 and 3, above.
6. Jumper B24 and any other of the system spares across the prototyping area of each backplane board.

C. Other Backplane Information

The prototyping area labeled E is for interfacing the OSI bus to other systems. Specifically, two 8T26 buffers can be placed there to interface to the KIM-1, the Motorola Development Kit, and other systems. For more specific information, request our App Note, "Interfacing to Other Systems."

The bus "spares" B13 through B23 are narrowed down at the areas marked D to allow easy cutting of the foils. This feature would be used to route special control signals to some of the boards. This feature will be used by some OSI boards also. The board can be mounted by enlarging the four holes labeled F and mounting the 480 Board against a firm support. If a conductive surface is to be used for support, the 480 Board should be backed by 1/4" masonite. Refer to the OSI App Note, "Construction Hints" for further details.

6502 System (All)

Address	Use
0000 up	User Page Zero Locations
00FF down	Monitor Page Zero Locations
0128 down	User Stack
0129 - 012F	Go Locations for 65A and 65V
0130	NMI Vector
01C0	IRQ Vector
01B0 - 01FF	65A Breakpoint
0200	Standard User Program Start Address (Cold Start)
0200 up	User Program
0FFF down	12S-1 Utilities
1FFF down	Deluxe Video Monitor Utilities

6800 Systems (68A 1K and 68V 1K)

Address	Use
0000 up	User Page Zero Location
0128 down	User Stack
0129 - 0131	Go Locations
01E0	NMI
01D0	IRQ
0200 up	User Program

6800 Systems (68A 8K and 68V 8K)

Address	Use
0000 up	User Page Zero Utilities
0100 up	User Program
1DXX	MIK Bug Linker Utilities
1EXX	Replaces A0XX (MIK Bug)
1FXX	Replaces 01XX (Superbug)

All Systems

Address	Use
AXXX	OSI-DOS 4K Buffer
BXXX CXXX	Reserved for Future OSI Boards
D000 up	440 Alphabetic Memory
D4XX up	440 Graphics Memory
DFFF	440 Keyboard Input
EXXX	Fast I/O
FXXX	Fully Decoded on Unmodified 400 Board
FBXX	430 I/O Board
FCXX	400 ACIA Interface
FDXX	400 PIA Interface
FEXX FFXX	OSI System Monitors