OSI APP NOTE

Subject: 6530 TIM Monitor   Number 1

The MOS Technology 6530 TIM Monitor can be used in place of a 6850 ACIA, OSI 65A Monitor and ½ of a 6820 PIA on the OSI 400 CPU boards using a 6502 Or 6501. The TIM provides a significant cost advantage for a very small system using an ASCII serial communications terminal such as an ASR33 teletype. However, the address space requirements and I/O subroutines of the TIM are somewhat incompatable with OSI software and system expansion techniques. The TIM user will be "on his own" when building a large system using the TIM Monitor.

TIM Monitor Installation

Proceed through Step 6 of standard construction details.

Step 7. Install sockets (for later expansion) or feed throughs at IC-7 and 8.

Step 8. Proceed with Step 8 of standard construction details.

Step 9. Omit installation of the ACIA socket and omit all ACIA clock steps. Install TIM 6530 at IC-A. Refer to the attached diagram for all TIM connections. Proceed with Step 10 and onward for the 6501 or 6502 processor.

Refer to the manuals accompanying the TIM for all operating instructions.
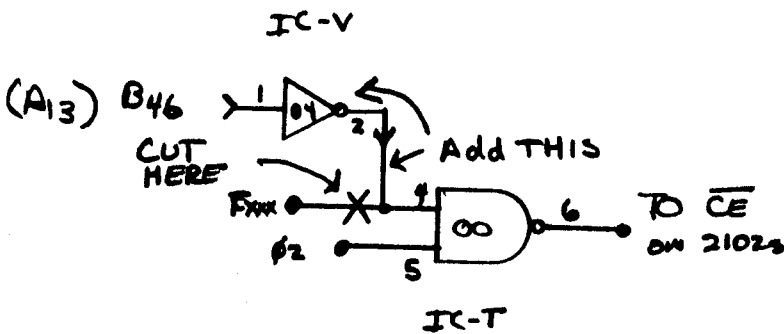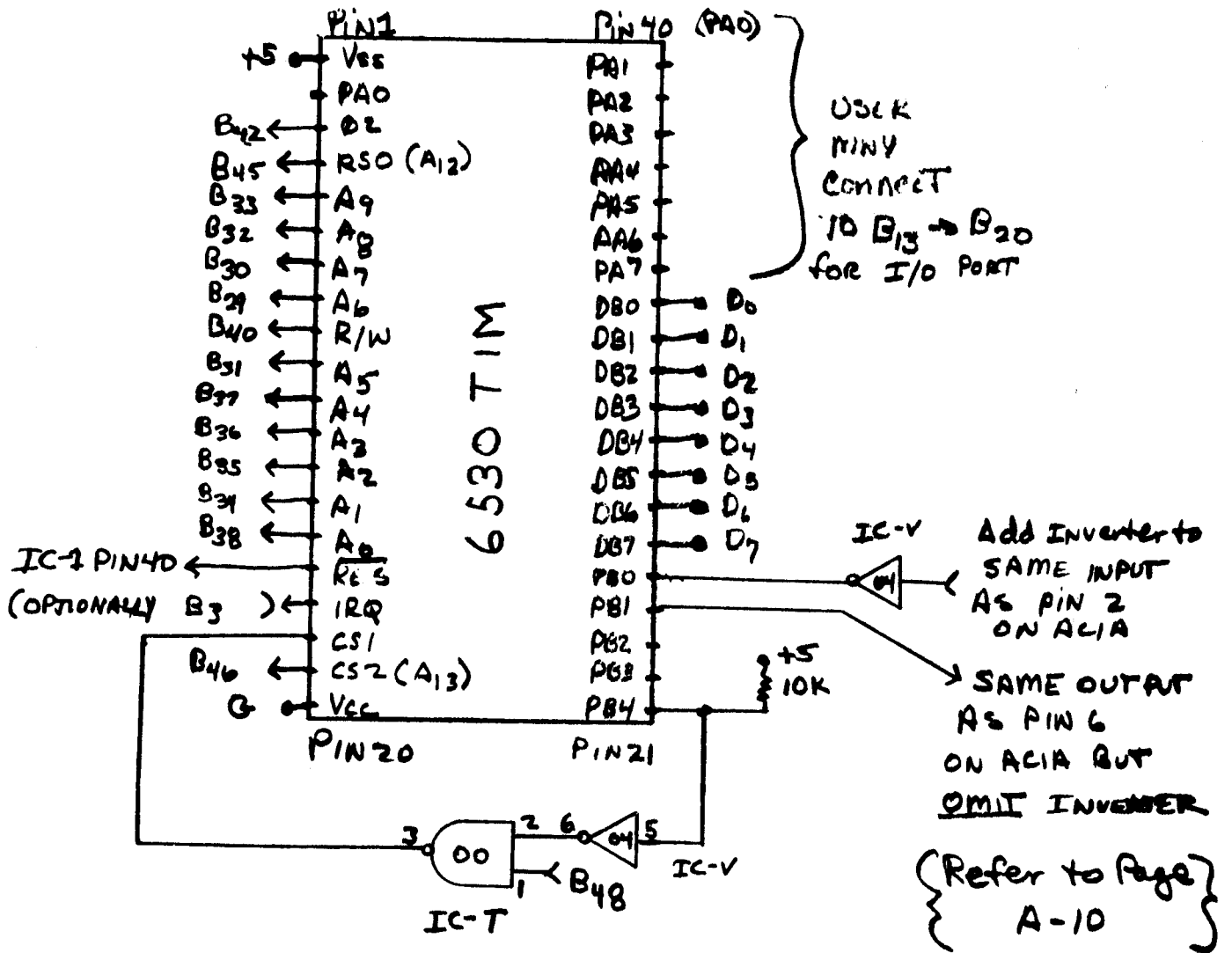
The 6530 TIM is available from:
MOS Technology, Inc.
950 Rittenhouse Road
Norristown, Pennsylvania 19401

6530-005

The 6530-005 is an unprogrammed version of the 6530 TIM. It has 16 parallel I/O lines like the 6820 PIA but also has a 64 word RAM and a programmable interval timer which can generate an IRQ. The 6530-005 is available directly from MOS Technology at a cost slightly higher than that of a 6820 PIA.

6530 KIM

Last fall, MOS Technology offered a 6530 programmed to operate with a hexadecimal keyboard and display. This part has been dropped from the MOS Technology price lists. The KIM provided an alternative to a front panel system for those without a teletype or other expensive computer terminal. The OSI 440 Video Graphics Board and 65V Monitor will provide alphanumeric display on a normal TV set at a cost just slightly above that of implementing the KIM Monitor. For this reason, and the obsolescence of the 6530 KIM, it is not recommended as a system component.

Pin1 Vss — +5

PAO

Φ2 — B42 ←

RS0 (A12) — B45 ←

A9 — B33 ←

A8 — B32 ←

A7 — B30 ←

A6 — B29 ←

R/W — B40 ←

A5 — B31 ←

A4 — B37 ←

A3 — B36 ←

A2 — B35 ←

A1 — B34 ←

A0 — B38 ←

R̄E̅S̅ — IC-1 PIN40 ←

IRQ — (OPTIONALLY B3) ←

CS1

CS2 (A13) — B46 ←

Vcc — G

Pin 20

6530 TIM

Pin 40 (PAO)

PB1

PA2

PA3

AA4

PA5

AA6

PA7

DB0 — • — D0

DB1 — • — D1

DB2 — • — D2

DB3 — • — D3

DB4 — • — D4

DB5 — • — D5

DB6 — • — D6

DB7 — • — D7

PB0

PB1

PB2

PB3

PB4

Pin 21

USCK MINY connect to B13 → B20 for I/O Port

IC-V — Add Inverter to SAME INPUT AS PIN 2 ON ACIA

+5 10K

SAME OUTPUT AS PIN 6 ON ACIA BUT **OMIT INVERTER**

{Refer to Page A-10}

3 —[00]— 2 — 6 ►o̅4 5

1 ► B48

IC-T — IC-V

IC-V

(A13) B46 ►1 o̅4 2

CUT HERE — Add THIS

Fxx • —X— 4 [00] 6 — TO C̄E̅ on 2102s

Φ2 • — 5

IC-T

NOTE —• termination INdicates foil connection

→ termination INdicates wire Jumper required.