BDV11 BUS TERMINATOR, BOOTSTRAP, AND DIAGNOSTIC ROM

Amps		Bus Loads		Cables
+5	+12	AC	DC	
1.6	.07	2	1	None

Standard Addresses

ROM Window	173000-173776
Page Control Reg.	177520
Scratch Pad Reg.	177522
Option Select Reg.	177524 (read only)
Display Reg.	177524 (write only)
Line Clock CSR	177546

Standard Vectors

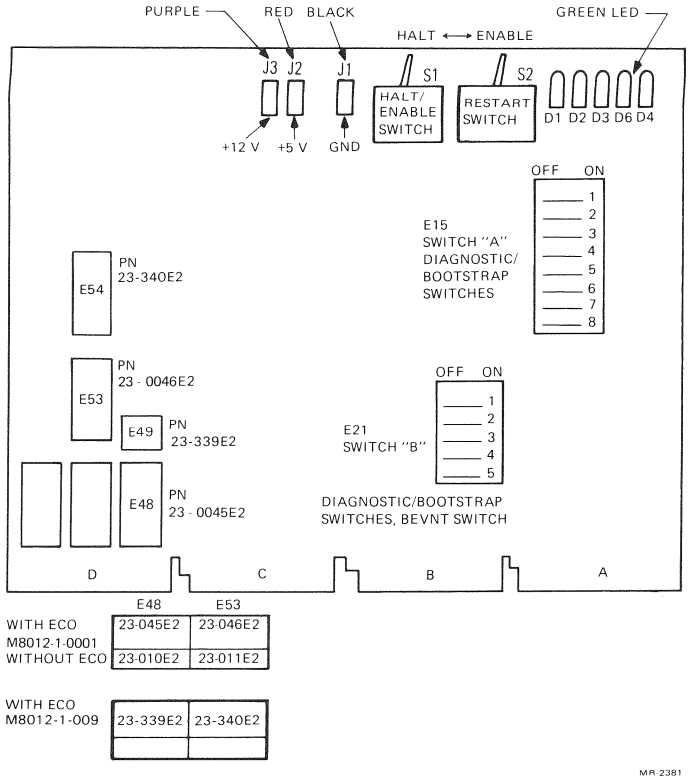
Line Clock	100

Diagnostic Programs

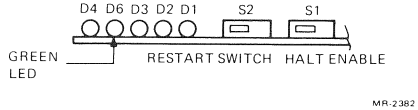
Refer to Appendix A.

Related Documentation

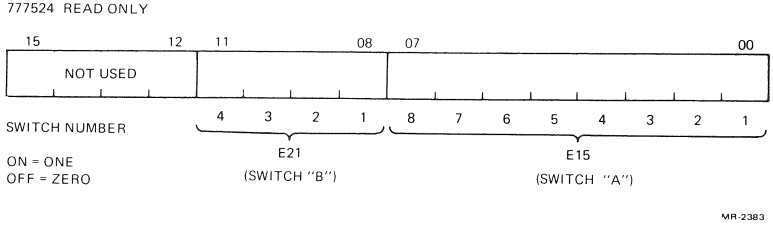
BDV11 Bus Terminator, Bootstrap, Diagnostic ROM Technical Manual (EK-BDV11-TM)
Field Maintenance Print Set (MP00489)
Microcomputer Interfaces Handbook (EB-20175-20)



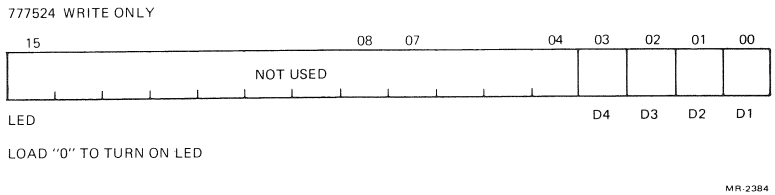
BDV11-A Switches and Indicators



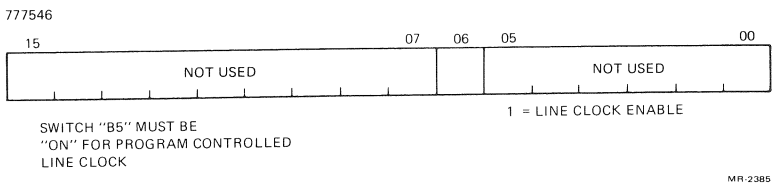
Diagnostic Light Display



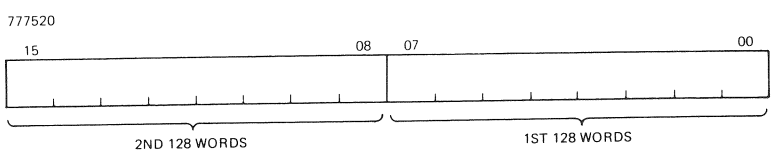
Switch Register



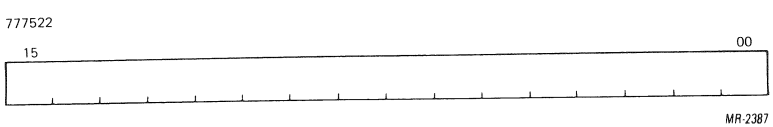
Display Register



Line Clock CSR



Page Control Register



Read/Write Register

BDV11 Hardware Registers

Register	Function	Bus Address
Page Control Register (PCR)	Controls mapping of ROM pages into physical ROM addresses. Cleared when power is turned on or when RESTART switch is activated. Sixteen bits.	177520. Word or byte byte addressable; can be read or written.
Read/Write Register	Maintenance register used for diagnostics. Cleared when power is turned on or when RESTART switch is activated. Sixteen bits.	177522. Word or byte byte addressable; can be read or written.
Switch Register	Used for maintenance and system configuration (selects diagnostic and/or bootstrap programs for execution). Bits 0-11 of the register (corresponding to E15-1 through E15-8 and E21-1 through E21-4, respectively) are associated with BDAL <0:11> L, respectively. When an individual switch of the register is closed (on), the corresponding BDAL signal is low (1). Twelve bits.	177524. Read-only register.
Display Register	Controls the diagnostic light display. Bits 0-3 of the register control LEDs D1-D4, respectively. When a bit is set, the corresponding LED is off; cleared (all lights on) when power is turned on or when RESTART switch is activated. Four bits.	177524. Word or byte addressable; write-only register.

BDV11 Hardware Registers (Cont)

Register	Function	Bus Address
Line Clock CSR	When cleared, this register clamps the BEVNT signal low (if BEVNT switch is closed). This action permits program control of the LSI-11 line time clock (LTC) function. Register cleared when power is turned on or when RESTART switch is activated. One bit.	177546. Word or byte addressable; write-only register.

(See ECO M8012-I-009.)

BDV11 (For ROMs 23-045E2 and 23-046E2 only)

Switch Settings and Mnemonics

For the discussion that follows, the M8012 switch E15 will be called "A" and E21, "B."

Switches A1 through B4 are defined as follows:

A1 ON Execute CPU tests on power-up or restart.
A2 ON Execute memory test on power-up or restart.
A3 ON DECNET BOOT - A4, A5, A6, A7 are used as arguments.

Device	A4	A5	A6	A7
DUV11	ON	OFF	OFF	OFF
DLV11-E	OFF	ON	OFF	OFF
DLV11-F	OFF	ON	OFF	ON

DLV11-E RCSR = 175610; DLV11-F RCSR = 176500.

A4 ON Console test and dialog (A3 OFF).
A4 OFF Turnkey BOOT dispatched by switch setting (A3 OFF).
Switches A5, A6, A7, A8, B1 are used as arguments.

Device	A5	A6	A7	A8	B1
Loop on Error	OFF	OFF	OFF	OFF	ON
RK05	OFF	OFF	OFF	ON	OFF
RL01	OFF	OFF	ON	OFF	OFF
RX01	OFF	ON	OFF	OFF	OFF
RX02	OFF	ON	ON	OFF	OFF
BDV11 ROM	ON	OFF	OFF	OFF	OFF

The BDV11 ROM BOOT uses the following switches as arguments. (X = don't care.)

ROM	B2	B3	B4
Extended DIAG	ON	X	X
2708s	OFF	ON	X
Program ROM	OFF	OFF	ON

All unused patterns or mnemonics will default to ROM BOOT if switch B2, B3, or B4 is ON.

If an unrecognized mnemonic or switch setting (A5 through B1) is encountered, the presence of additional ROM is checked (by checking B2, 3, 4) and if present, the ROM BOOT is envoked.

If an unrecognized switch setting is encountered, a copy of the switches is placed in location 2 with bit 15 set.

If no additional ROM exists, the switch checking routine will halt or the mnemonic routine will reprompt.

If the console test is selected, the console test prompts with:

ZZK Where ZZ is the decimal multiple of 1024.
START? Words of RAM found in the system.

Allowed responses are a two-character mnemonic with a one-digit octal unit number, or one of two special, single-character mnemonics. The response must be followed by a return. The special single-character mnemonics are:

Y Use switch settings to determine boot device; or,
N HALT. Enter microcode ODT.

The two-character mnemonics are as follows. "N" is a digit from 1 to 7 indicating the unit number of the device.

DKN	RK05 bootstrap
DLN	RL01 bootstrap
DXN	RX01 bootstrap
DYN	RX02 bootstrap

BDV11 HALT/ENABLE, RESTART, AND BEVNT SWITCHES

HALT/ENABLE Switch

When this switch is in the ENABLE position, the LSI-11 CPU can operate under program control. If the switch is placed in the HALT position, the CPU enters the halt mode and responds to console ODT commands. While in the halt mode, the CPU can execute single instructions, facilitating maintenance of the system. Program control is re-established by returning the switch to the ENABLE position and entering a "P" command at the console terminal (providing the contents of register R7 were not changed). Refer to chapter 2 of the *Microcomputer Handbook* (1977-1978) for a description of console ODT command usage.

RESTART Switch

When the RESTART switch is cycled, i.e., moved from one side to the other and back, the CPU automatically carries out a power-up sequence. Thus, the system can be rebooted at any time for maintenance purposes.

BEVNT L Switch

Contact 5 of dip-socket switch E21 is the BEVNT L switch. When the switch is off (open) the LSI-11 bus BEVNT L signal can be controlled by the power-supply-generated LTC signal. When the switch is on (closed), the LTC function is program controlled; i.e., a single-bit write-only register in the logic (address 177546, bit 6) clamps BEVNT L low when the register is cleared. (The register is automatically cleared when the power is turned on or when the RESTART switch is cycled.) The KW11-L line time clock option also uses bit 6 as the enable bit.

POWER OK LED and Tip Jacks

This green LED is lighted when the +12 Vdc supply voltage is greater than +10 V and the +5 Vdc supply voltage is greater than +4 V. The +12 Vdc voltage and the +5 Vdc voltage can be measured at the tip jacks as indicated below. (Both J2 and J3 have a 560 Ω resistor in series to prevent damage from a short circuit; use at lease a 20,000 Ω V meter to measure the voltage.)

Jack	Color	Voltage
J1	Black	Ground
J2	Red	+5 Vdc
J3	Purple	+12 Vdc

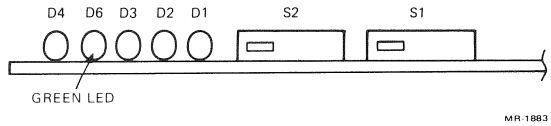
Secondarily, the LED indicates the octal point for the diagnostic light display.

The BDV11 (M8012) is the new bootstrap module for the PDP-11/03s. It is a quad module and it has 2K words of diagnostics in ROM installed on the board. The failures of these diagnostics are indicated by the HALT address in the ROM and by the state of the error lights on the board.

The "Diagnostic LED Error Display" table provides a cross-reference between the indications in the error lights and the failing system function. The "BDV11 Diagnostic Error Addresses" table provides a cross-reference between the HALT PC and the failing system function. (The HALT PC will be displayed on the console terminal.)

Diagnostic LED Error Display

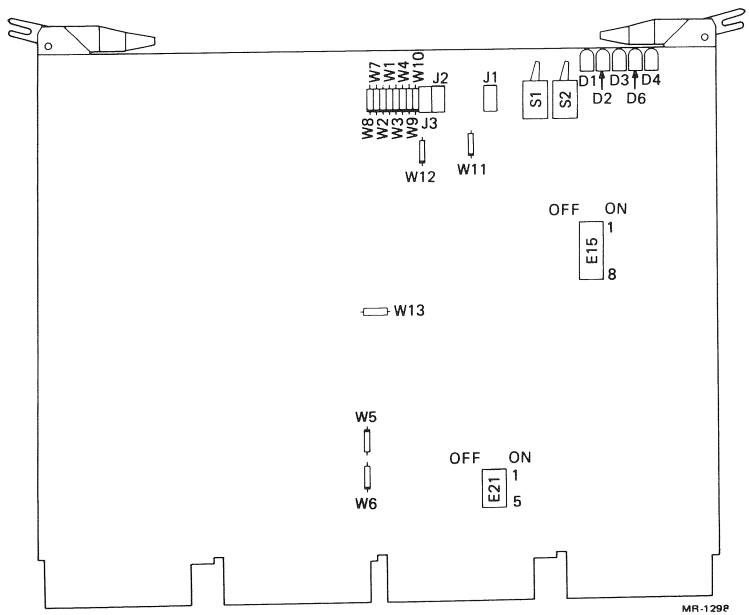
D4 Red	D6 Green DC OK	D3 Red	D2 Red	D1 Red	Comments
X	OFF	X	X	X	+12 Vdc or +5 Vdc is bad.
OFF	ON	OFF	OFF	ON	CPU test error or fault, or configuration error.
OFF	ON	OFF	ON	OFF	Memory test error; register R1 points to bad location.
OFF	ON	OFF	ON	ON	Console serial line unit does not transmit.
OFF	ON	ON	OFF	OFF	Console terminal test waiting for response from operator on keyboard.
OFF	ON	ON	OFF	ON	Load device status error.
OFF	ON	ON	ON	OFF	Secondary bootstrap code incorrect. NOP instruction is not in location 000000; the medium is probably bad.
OFF	ON	ON	ON	ON	DECNET waiting for response from host computer.
ON	ON	OFF	OFF	OFF	DECNET received DONE FLAG set.
ON	ON	OFF	OFF	ON	DECNET message received.
ON	ON	OFF	ON	OFF	ROM BOOTSTRAP error.
ON	ON	ON	ON	ON	HALT switch is ON, unable to run (check computer and BDV11 HALT switch); or power-up mode is wrong; or system is hung.



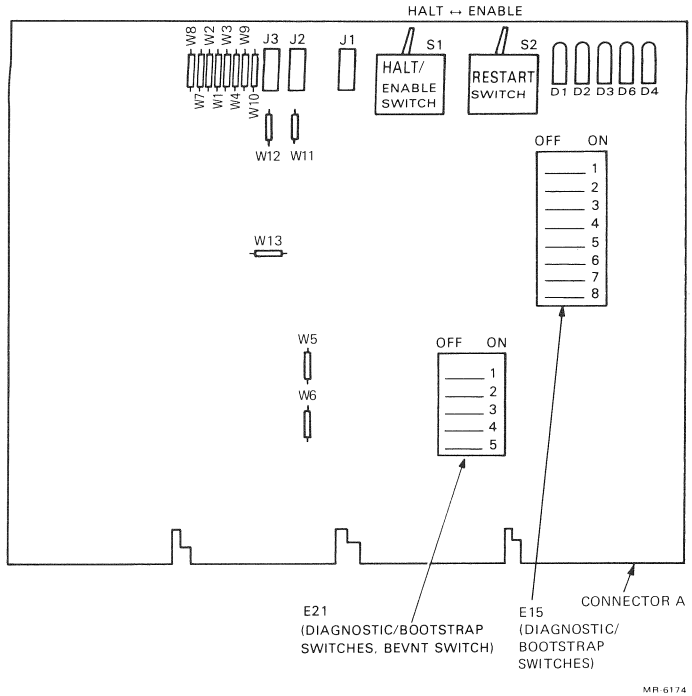
Diagnostic LED Error Display

BDV11 Diagnostic Error Addresses

Error Address	Cause of Error
173022	Memory error 1. Write address into itself.
173040	Serial line unit switch selection incorrect; error in switches.
173046	Serial line unit error. CSR address for selected device in error. Check CSR for selected device in floating CSR address area.
173050	CPU error 1. Register R0 contains address of error.
173052	Memory error 2. Data test failed.
173106	Memory error 3. Write and read bytes failed.
173202	ROM loader error. Checksum on data block.
173240	CPU error 4. R0 contains address of error.
173366	ROM loader error. Checksum on address block.
173402	ROM loader error. Jump address is odd.
173532	RL device error.
173634	CPU error 3. R0 points to cause of error.
173642	A "NO" typed in console terminal test.
173656	Switch mode HALT. A match was not made with switches.
173656	RK device error
173670	Console terminal test. No DONE flag.
173706	CPU error 2. R0 points to cause of error.
173712	RX device error



BDV11 Switch and Jumper Locations



BDV11 Switches and Indicators

Socket Selection Logic

The socket selection logic determines which pair of sockets responds to the ROM address signals. (Although the ROMs in the sockets actually respond, it is said, for ease of explanation, that the sockets respond).

Jumpers are inserted selectively in positions W1-W4 and W9-W12. These jumpers cause the PCR page numbers and the selection signals (and, therefore the sockets) to be related in definite ways. Group A in the "BDV11 Selection Signals/Sockets" table indicates that PCR pages are assigned to specific ROM sockets. This is true within the confines of the BDV11 module shipped by DIGITAL. On such a module, jumpers W1-W4 and W9-W12 are arranged as indicated under Group A in the table. Thus, the PCR pages 0-17, for example, cause selection signal SB1 L to be asserted, and SB1 L causes sockets XE53 and XE48 to respond to address signals A<0:10> H. Other combinations of jumpers are possible, as indicated by Groups B through G in the table. Note that each selection signal always selects the same pair of sockets; however, the relation of PCR pages to selected sockets varies with jumper configuration.

BDV11 Selection Signals/Sockets

Group	W1	W2	W3	W4	W9	W10	W11	W12	PCR Page	Primary Selection Signal	Addresses (A<0:14>H)	Sockets Selected
A	R	I	I	R	I	R	R	I	0-17	SB1 L	0K-2K	XE53/XE48
									20-37	SB2 L	2K-4K	XE58/XE44
									40-47	SE1 L	4K-5K	XE57/XE40
									50-57	SE2 L	5K-6K	XE52/XE36
									360-377	SP1 L	30K-32K	XE39/XE50
									340-357	SP2 L	28K-30K	XE43/XE46
									320-337	SP3 L	26K-28K	XE47/XE42
									300-317	SP4 L	24K-26K	XE51/XE38
									260-277	SP5 L	22K-24K	XE55/XE37
									240-257	SP6 L	20K-22K	XE60/XE41
									220-237	SP7 L	18K-20K	XE59/XE45
									200-217	SP8 L	16K-18K	XE54/XE49
B	*	*	*	*	I	R	I	R	40-57	SB1 L	4K-6K	XE53/XE48
									60-77	SB2 L	6K-8K	XE58/XE44
									0-7	SE1 L	0K-1K	XE57/XE40
									10-17	SE2 L	1K-2K	XE52/XE36
C	*	*	*	*	R	I	R	I	200-217	SB1 L	16K-18K	Ibid.
									220-237	SB2 L	18K-20K	
									240-247	SE1 L	20K-21K	
									250-257	SE2 L	21K-22K	
D	*	*	*	*	R	I	I	R	240-257	SB1 L	20K-22K	Ibid.
									260-277	SB2 L	22K-24K	
									200-207	SE1 L	16K-17K	
									210-217	SE2 L	17K-18K	

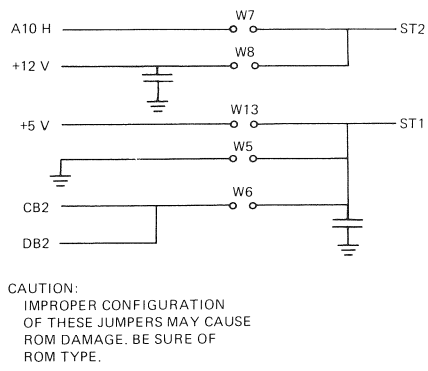
BDV11 Selection Signals/Sockets (Cont)

Group	W1	W2	W3	W4	W9	W10	W11	W12	PCR Page	Primary Selection Signal	Addresses (A<0:14>H)	Sockets Selected
E	I	R	I	R	*	*	*	*	270-277	SP1 L	23K-24K	XE39/XE50
									250-257	SP2 L	21K-22K	XE43/XE46
									230-237	SP3 L	19K-20K	XE47/XE42
									210-217	SP4 L	17K-18K	XE51/XE48
									260-267	SP5 L	22K-23K	XE55/XE37
									240-247	SP6 L	20K-21K	XE60/XE41
									220-227	SP7 L	18K-19K	XE59/XE45
									200-207	SP8 L	16K-17K	XE54/XE49
F	R	I	R	I	*	*	*	*	160-177	SP1 L	14K-16K	Ibid.
									140-157	SP2 L	12K-14K	
									120-137	SP3 L	10K-12K	
									100-117	SP4 L	8K-10K	
									60-77	SP5 L	6K-8K	
									40-57	SP6 L	4K-6K	
									20-37	SP7 L	2K-4K	
									0-17	SP8 L	0K-2K	
G	I	R	R	I	*	*	*	*	70-77	SP1 L	7K-8K	Ibid.
									50-57	SP2 L	5K-6K	
									30-37	SP3 L	3K-4K	
									10-17	SP4 L	1K-2K	
									60-67	SP5 L	6K-7K	
									40-47	SP6 L	4K-5K	
									20-27	SP7 L	2K-3K	
									0-7	SP8 L	0K-1K	

I = inserted; R = removed.

ROM Sockets Logic

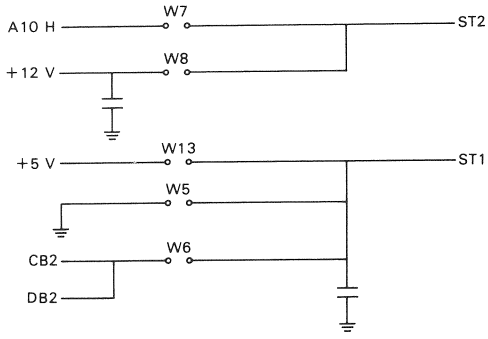
The following figure represents the ROM sockets and shows the address signals and enabling signals for each functional group of sockets. The diagnostic/bootstrap ROM sockets (which are selected by signals SB1 L and SB2 L) are supplied with 11 address bits, since these sockets are reserved for 2K-word ROMs. The EPROM sockets (selected by signals SE1 L and SE2 L) are reserved for 1K ROMs; therefore, these sockets are supplied with 10 address bits. The system ROM sockets can be occupied by either 2K ROMs or 1K ROMs; five jumpers on the BDV11 module permit ROMs of either size to be used.



The following figure shows how these five jumpers control the selection signals for the system ROM sockets, and relates the jumpers to the types of ROM that can be used in the BDV11. (If ROMs other than 8316E, 2716, and 2708 are used, do not alter configuration. See Caution.)

CAUTION

Improper configuration of these jumpers may cause ROM damage. Be sure of ROM type.



ROM TYPE	JUMPERS INSERTED[1]				
	W5	W6	W7	W8	W13
2708[2]	R	I	R	I	R
2716	R	R	I	R	I
8316E[3]	I	R	I	R	R
8316E[4]	R	R	I	R	I

1. I=INSERTED; R=REMOVED
2. CB2 AND DB2 MUST BE SUPPLIED WITH EXTERNAL -5V POWER.
3. CHIP SELECT SIGNALS MUST BE PROGRAMMED AS FOLLOWS:

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
LOW	LOW	LOW

4. CHIP SELECT SIGNALS MUST BE PROGRAMMED AS FOLLOWS:

$\overline{CS1}$	$\overline{CS2}$	$\overline{CS3}$
LOW	LOW	HIGH

MA-1351