Amdahl 470 Systems

MANAGEMENT SUMMARY

The marketing strategy of IBM, although effective most of the time, has not prevented the company founded by Dr. Gene Amdahl from continuing expansion of its user base through the introduction of technologically advanced and innovative systems. Since its inception, the Amdahl Corporation has announced new products when necessary to keep abreast or ahead of IBM. Although Amdahl's original products were more powerful than any competitive system from IBM, the firm now markets processors which compete head on with IBM in the 303X arena. The latest Amdahl product, the 470V/7B for example, is designed to compete directly against the newly announced IBM 3033N system.

A summary of the product line includes the 470V/5, operating at about the speed of the 168-3/3032; the 470V/5-II with 10 percent greater performance than the 470V/5; the 470V/6, the original Amdahl product, with a performance factor rated at 1.3 to 1.5 times the 168-3/3032; the 470V/6-II, offering 5 to 15 percent greater performance than the 470V/6; the 470V/7, providing 1.2 to 1.4 times the power of the 3033; the 470V/7A, capable of 80 percent of the performance of the 470V/7; the 470V/7B, with 60 to 65 percent of the performance of the 470V/7; and the 470V/8, providing 20 to 30 percent more speed than the 470V/7.

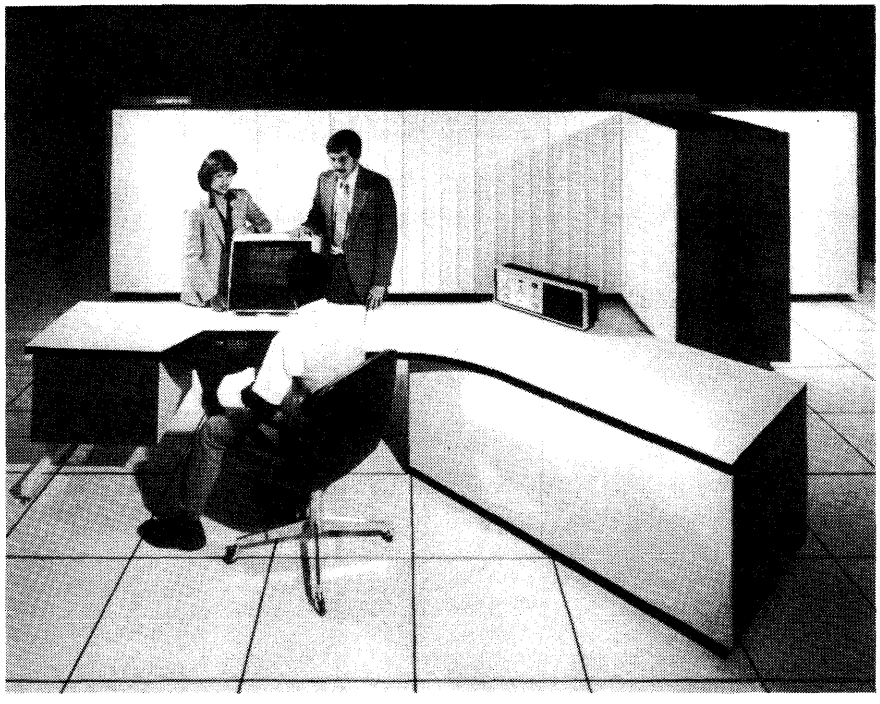
The Amdahl 470 configurations consist of a central processor unit with 8, 12, or 16 integrated input/output channels, a minicomputer-based system console with CRT display, from 4 to 16 million bytes of main memory, ➢

The Amdahl 470 product line of IBM plug-compatibles now stands at eight processors, ranging from the 470V/5 to the large-scale 470V/8. All the processors offer options of up to 16 channels and up to 8 or 16 megabytes of memory. The Amdahl systems execute any System/360 or System/370 software and utilize and peripheral devices that are compatible with these IBM processors.

CHARACTERISTICS

MANUFACTURER: Amdahl Corporation, 1250 East Argues Avenue, Sunnyvale, California 94086. Telephone (408) 735-4011.

Amdahl is a high technology company employing 3300 individuals engaged in the design, development, manufacture, marketing, and servicing of large scale IBM 370/303X-compatible processors. In a second but equally important area, Amdahl is engaged in the upgrading of system software performance to increase productivity of their 470 line of processors. The company maintains 50 marketing and support offices in the United States within six geographic regions. Foreign marketing and support offices are provided through subsidiaries in Canada, Belgium, Denmark, France, West Germany, the Netherlands, Norway, Sweden, Switzerland, and the United Kingdom, and through a distributor in Australia. Manufacturing facilities are located in the United States and Ireland. Amdahl systems are employed in applications including industry, finance and banking, transportation and distribution, education, government, manufacturing, data services, communications and utilities, and insurance and health services. ➤



Under the covers of the 470 console lie an independent processing system. Immediately to the operators left is a floppy disk storage area; to his right under the table cabinet is a fixed head disk drive used by the console operating system, a standard channel interface between computer and console operating system, a standard channel interface between computer and console for console operation, an independent minicomputer console processor, floppy disk drives for loading diagnostic programs direct computer-to-console interface for direct diagnostics on the 470 central system, and a modem to connect to the AMDAC remote diagnostic service.

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CHARACTERISTICS OF THE AMDAHL 470 SYSTEMS

	470V/5	470V/5-II	470V/6	470V/6-II
SYSTEM CHARACTERISTICS				
Relative performance to 168-3/3032	0.9 to 1.1	1.0 to 1.2	1.3 to 1.5	1.4 to 1.6
Date announced	3/77	10/78	9/74	2/77
Date of first delivery	9/77	4/79	6/75	8/77
Production status	Active	Active	No new prod.	Active
Number of processors	1	1	1	1
Multiprocessor configurations	No	No	No	No
Principal operating systems	OS/VS1, SVS, MVS, VM/370	OS/VS1, SVS, MVS, VM/370	OS/VS1, SVS, MVS, VM/370	OS/VS1, SVS, MVS, VM/370
Upgradable to:	470V/5-II	470V/6-II	470V/6-II	—
	470V/6	—	—	—
	470V/6-II	—	—	—
MAIN STORAGE				
Type	Dynamic NMOS	Dynamic NMOS	Dynamic NMOS	Dynamic NMOS
Cycle time, nanoseconds per 32 bytes	325	325	325	325
Bytes fetched per cycle	4	4	4	4
Interleaving	2 or 4 ways	2 or 4 ways	2 or 4 ways	2 or 4 ways
Minimum capacity bytes	4,194,304	4,194,304	4,194,304	4,194,304
Maximum capacity bytes 2M	8,388,608	8,388,608	8,388,608	8,388,608
Increment size (field upgrade)	2,097,152	2,097,152	2,097,152	2,097,152
Error detection and correction	9 bits/16 bytes	9 bits/16 bytes	9 bits/16 bytes	9 bits/16 bytes
PROCESSOR				
Cycle time, nanoseconds	32.5	32.5	32.5	32.5
Translation look aside buffer	256 entries	256 entries	256 entries	256 entries
Segment table origin stack	32 entries	32 entries	32 entries	32 entries
Instruction lookahead	4 levels	4 levels	4 levels	4 levels
High speed buffer				
Type	Bipolar RAM	Bipolar RAM	Bipolar RAM	Bipolar RAM
Cycle time, nanoseconds	65 for 4 bytes	65 for 4 bytes	65 for 4 bytes	65 for 4 bytes
Capacity, bytes	16,384	32,768	16,384	32,768
I/O Channels				
Number standard	8 (all types)	8 (all types)	8 (all types)	8 (all types)
Number optional	4 or 8 (all types)	4 or 8 (all types)	4 or 8 (all types)	4 or 8 (all types)
Subchannels per channel	256	256	256	256
Total subchannels	1,024	1,024	1,024	1,024
Channel to channel adapter	Yes	Yes	Yes	Yes
Block multiplexer, bytes per second	1.9M	1.9M	1.9M	1.9M
With two-byte interface	3.8M	3.8M	3.8M	3.8M
Selector, bytes per second	1.9M	1.9M	1.9M	1.9M
With two-byte interface	3.8M	3.8M	3.8M	3.8M
Byte multiplexer, bytes per second	110K	110K	110K	110K
Burst mode	1.9M	1.9M	1.9M	1.9M
Aggregate data rate, bytes per second	14M	14M	14M	14M

and a power distribution unit. Central processor functions are performed by four independent functional units: a Storage Unit that controls accesses to main memory and includes both virtual address translation hardware and a cache memory; an Instruction Unit for controlling instruction interpretation and execution; an Execution Unit that performs the arithmetic, logic, and data manipulation functions of instruction execution; and a Channel Unit that interprets and executes input/output instructions and interfaces with the standard control unit interface that can communicate with any System/360- or System/370-compatible peripheral equipment. Operation of all the functional units can be overlapped, and four-way interleaving can be performed on accesses to main memory. The degree of interleaving is partially dependent on the processor model.

Amdahl Corporation was the first company to develop and produce an IBM plug-compatible mainframe com-

MODELS: Amdahl 470V/5, 470V/5-II, 470V/6, 470V/6-II, 470V/7B, 470V/7A, 470V/7, and 470V/8.

DATE ANNOUNCED: See table.

DATE OF FIRST DELIVERY: See table.

NUMBER INSTALLED TO DATE: Over 203 worldwide.

DATA FORMATS

All data formats, instruction formats, and other architectural features completely follow IBM System/370 architecture.

BASIC UNIT: 8-bit bytes. Each byte can represent 1 alphanumeric character, 2 BCD digits, or 8 binary bits. Two consecutive bytes form a "halfword" of 16 bits, while 4 consecutive bytes form a 32-bit "word."

FIXED-POINT OPERANDS: Can range from 1 to 16 bytes (1 to 31 digits plus sign) in decimal mode; 1 halfword (16 bits) or 1 word (32 bits) in binary mode.

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CHARACTERISTICS OF THE AMDAHL 470 SYSTEMS

	470V/7	470V/7A	470V/7B	470V/8
SYSTEM CHARACTERISTICS				
Relative performance to 168-3/3032	2.1 to 2.4	1.7 to 1.9	1.4 to 1.6	2.6 to 3.0
Date announced	3/77	8/79	11/79	10/78
Date of first delivery	8/78	9/79	3/80	9/79
Production status	Active	Active	Active	Active
Number of processors	1	1	1	1
Multiprocessor configurations	No	No	No	No
Principal operating systems	OS/VS1, SVS, MVS, VM/370	OS/VS1, SVS, MVS, VM/370	OS/VS1, SVS, MVS, VM/370	MVS, VM/370
Upgradable to:	470V/8	470V/7	470/7A	—
	—	—	—	—
	—	—	—	—
MAIN STORAGE				
Type	Dynamic NMOS	Dynamic NMOS	Dynamic NMOS	Dynamic NMOS
Cycle time, nanoseconds	290	290	290	260
Bytes fetched per cycle	4	4	4	4
Interleaving	4-	4 way	4 way	4 way
Minimum capacity bytes	4,194,304	4,194,304	4,194,304	4,194,304
Maximum capacity bytes	16,777,216	16,777,216	8,388,608	16,777,216
Increment size (field upgrade)	4,194,304	4,194,304	4,194,304	4,194,304
Error detection and correction	8 bits/8 bytes	8 bits/8 bytes	8 bits/8 bytes	8 bits/8 bytes
PROCESSOR				
Cycle time, nanoseconds	29	29	29	26
Translation lookaside buffer	512 entries	512 entries	512 entries	512 entries
Segment table origin stack	128 entries	128 entries	128 entries	128 entries
Instruction lookahead	4 levels	4 levels	4 levels	4 levels
High speed buffer				
Type	Bipolar RAM	Bipolar RAM	Bipolar RAM	Bipolar RAM
Cycle time, nanoseconds	58 for 4 bytes	58 for 4 bytes	54 for 4 bytes	52 for 4 bytes
Capacity, bytes	32,768	32,768	32,768	65,356
I/O Channels				
Number standard	12 (all types)	8 (all types)	8 (all types)	12 (all types)
Number optional	4 (all types)	4 or 8 (all types)	4 or 8 (all types)	4 (all types)
Subchannels per channel	256	256	256	256
Total subchannels	2,048	2,048	2,048	2,048
Channel to channel adapter	Yes	Yes	Yes	Yes
Block multiplexer, bytes per second	2.0M	2.0M	2.0M	2.0M
With two-byte interface	4.0M	4.0M	4.0M	4.0M
Selector, bytes per second	2.0M	2.0M	2.0M	2.0M
With two-byte interface	4.0M	4.0M	4.0M	4.0M
Byte multiplexer, bytes per second	110K	110K	110K	110K
Burst mode	2.0M	2.0M	2.0M	2.0M
Aggregate data rate, bytes per second	18M	18M	18M	18M

puter. The company, formed in 1971 by Dr. Gene Amdahl, delivered its first processor, the 470V/6, in June 1975.

The original Amdahl 470 was intended to be a real-memory system targeted at IBM's System/370 Model 165. The target moved, however, with IBM's announcement of the virtual-memory 370/168 in August 1972, and Amdahl modified its system design to incorporate virtual-memory hardware, enabling the new system to compete with IBM's latest technology. The system that resulted from this shift in direction, the 470V/6, featured about 1.5 times the performance level of the IBM 370/168 at a similar price, while occupying only one-third of the space required by the IBM counterpart. Further, it operates in an ordinary air-conditioned environment with no requirements for the liquid cooling facilities that are necessary for very large IBM systems. The two systems have one requirement in common: a motor-generator set for the

FLOATING-POINT OPERANDS: 1 word, consisting of 24-bit fraction and 7-bit hexadecimal exponent, in "short" format; 2 words, consisting of 56-bit fraction and 7-bit hexadecimal exponent, in "long" format; for 4 words in "extended precision" format.

INSTRUCTIONS: 2, 4, or 6 bytes in length, which usually specify 0, 1, or 2 memory addresses respectively.

INTERNAL CODE: EBCDIC (Extended Binary-Coded Decimal Interchange Code).

MAIN STORAGE

STORAGE TYPE: Dynamic NMOS.

CYCLE TIME: Memory cycle times are given in the table. Stated rates are for a 32-byte "line". However, since all memory is interleaved, effective cycle times is significantly reduced depending on the degree of interleaving. For example, an effective cycle time around 163 nanoseconds is achieved on the 470V/5 through 470V/6-II using four way interleaving.

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400-Hertz system power is needed for both the Amdahl 470V/6 and the IBM 370/168. (The 470 can also use a static frequency coverter.)

Amdahl Corporation was founded by computer wizard Gene M. Amdahl, principal designer of the IBM System/360 and subsequently a director of IBM's advanced systems laboratory and an IBM Fellow, the company's highest scientific position. Its original investors included Heizer Corporation, Fujitsu Ltd., and Nixdorf Computer AG. Nixdorf Computer, however, recently divested itself of its shares in Amdahl Corporation.

Fujitsu, in addition to being the largest investor in Amdahl, holding 26.7 percent of the corporation's common stock, has manufactured a substantial portion of the subassemblies used in the 470 systems. However, Amdahl has increased its manufacturing facilities and now makes most subassemblies in-house. Fujitsu also manufactures and markets, in Japan, an M-series computer system. Under the present agreements with Amdahl, Fujitsu could begin marketing the M-series systems in the U.S. and become another competitor in the IBM plug-compatible mainframe race.

The Amdahl 470 design is based on the System/370 architecture. It achieves its superior performance through the use of the latest in super-fast integrated circuit technology and, to a lesser extent, from central processor architectural optimization that provides for more efficient operation of the high-speed buffer memory and the virtual-storage address translation hardware, and permits extensive overlapping of input/output operations and instruction execution in the central processor.

Large-scale integrated (LSI) semiconductor circuits are used extensively throughout the system, resulting in increased processing speeds, higher reliability, and reduced space and cooling requirements. The central processor uses an LSI version of bipolar emitter-coupled logic (ECL) with chip speeds in the area of 600 picoseconds (trillionths of a second), and has a CPU cycle time of 32.5 nanoseconds. The 470V/7 cuts this time to 29 nanoseconds, while the 470V/8 boasts a cycle time of 26 nanoseconds.

Main memory in the 470 processors is metal oxide semiconductor (MOS) LSI circuits with a cycle time of 260 to 325 nanoseconds (depending on processor model), while ultra-high speed components are used in the cache-like buffer memory with a 52 to 65 nanosecond cycle time for 4-byte access, depending on processor model. Buffer loading from main memory is performed in 32-byte blocks. Using four-way main storage interleaving capabilities, a maximum data transfer rate of one 32-byte "line" per 163 nanoseconds can be achieved between the high-speed buffer and main memory on the 470V/5 through 470V/6-II models.

At the time when development began on the Amdahl system, economically practical LSI technologies were not

CAPACITY: See table. Memory increments of 4,194,304 bytes are standard on the 470V/7 Series and the 470V/8 while 2,097,152 byte increments are standard on the 470V/5s and 470V/6's. Memory units are equipped with their own power supply.

CHECKING: Error checking and correction (ECC) circuitry in main memory performs automatic correction of all single-bit errors and detection of all double-bit and most other multiple-bit memory errors. See table for number of bits per byte group added for ECC.

A Configuration Control Register, associated with each two-million-byte storage unit, maintains a map of the assignment of main storage address space for that storage unit. In the event of an unrecoverable memory error, the memory module can be removed from operation and the remaining memory reconfigured for continuous system operation.

In addition, a parity check is performed on all data transferred between main memory and the High-Speed Buffer. A separate parity check is also made on storage keys, which are used to implement storage protection and to record references and modifications to main storage.

STORAGE PROTECTION: Storage protection facilities are comparable to those implemented in the IBM System/370.

RESERVED STORAGE: The 470 processors reserve an area in lower memory for such purposes as interrupt handling routines, CPU ID, channel ID, and machine check logouts.

STORAGE CONTROL UNIT (S-UNIT): The Storage Control Unit, or S-Unit, handles all requests for data from main storage made by the CPU and the channels. An internal priority structure is used to resolve conflicts resulting from multiple concurrent requests for access to main memory. The internal priority structure of the S-Unit has the following five priority levels, in descending order: Internal High (including ECC handling), Channel Unit High, Central Processing Unit, Channel Unit Low, and Internal Unit Low (such as instruction prefetch). Normally, the central processor unit is given higher priority than a channel except when a channel issues a high-priority request. The Storage Control Unit locates the requested data either in the High-Speed Buffer or in main memory and includes a dynamic address translation facility for translating program-specified virtual addresses into real-memory addresses.

All Amdahl processors include a High-Speed Buffer (HSB) that is organized as a set associative memory composed of from two to eight partitions. Each partition is organized into 32-byte lines that can be addressed on a single-word or double-word basis.

The 470V/5 and 470V/6 have 256 32-byte lines in each partition. The 470V/5-II and 470V/6-II have 512 32-byte lines in each partition. The 470V/7, 470V/7A, and 470V/7B all have eight equal partitions with each partition having 128 32-byte lines. The 470V/8 is partitioned four ways where each partition has 512 32-byte lines. Partitioning allows the system to bypass buffer errors by reconfiguring out a buffer section. The 470V/8 HSB incorporates a special prefetching technique which predicts the next most logical consecutive data to be called into the buffer from main storage and then moves the data into the buffer.

For systems control programs using 2K pages, the HSB operates in 16K mode only. this applies to the 470V/5-II, 470V/6-II, 470V/7B, 470V/7A, 470V/7, and 470V/8.

Data is transferred between the buffer and the central processing unit in groups of 4 bytes per cycle and is brought

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available to produce circuit chips with the density and speed required to implement the Amdahl concepts. As a result, all of the circuitry, plus the manufacturing techniques, test equipment, and chip interconnection methods, have been specially designed by Amdahl engineers.

The LSI chips developed for the Amdahl 470V's measure 154 thousandths of an inch square, are 10 mils thick, and have a maximum capacity of about 100 circuits. The LSI chips are mounted on a multi-chip carrier, which is the field-replaceable unit of the system. Each carrier has a maximum capacity of about 4200 circuits. Thus, all 150,000 circuits comprising the 470V/6-II system can be housed on 51 multi-chip carriers (MCCs), resulting in a system requiring an estimated one-third of the floor space occupied by an IBM System/360 Model 168 with its associated channels. Similar space reductions are possible with the 470 processors. The 470V/7 for example, has 60 MCCs.

The Amdahl circuits also require significantly less power than that consumed by standard ECL circuitry, resulting in significantly reduced cooling requirements for the system. All 470 systems are air-cooled, and a cooling stub is bonded to the surface of each LSI chip carrier to conduct heat into the air flow.

The miniaturization of the 470 circuitry substantially reduces the number of wiring interconnections required in the system, resulting in potentially fewer system failures. Additional circuitry on each subassembly also allows some 17,000 key logic points in the system to be examined and exercised by diagnostic programs under control of the system console. Remote diagnostic services are also available through a modem supplied with the system console. Other reliability features incorporated in the design include instruction retry, error checking and correction (ECC) circuitry in main memory, and the ability to recover from high-speed buffer and main memory failures by configuring out the malfunctioning portions of the buffer and main memory.

Although the basic concept underlying the 470 system design is to produce an extremely fast but architecturally simple computer system, sophisticated modifications have been made to several key functional components to achieve more efficient operation. The high-speed buffer, for example, uses a "non-store-through" technique, permitting data to be modified in the buffer without updating main storage. Main storage is updated only when the data is written back to main storage to provide space for new data. In addition, Amdahl has engineered a number of probe points into the hardware to facilitate the use of hardware monitors and has recently introduced a Hardware Measurement Interface (HMI). The HMI can be used with most commercial hardware monitors.

Instruction execution is performed in a "pipeline" structure which allows the execution of up to six instructions to occur concurrently. In addition, although the Amdahl Dynamic Address Translation (DAT) feature provides

into the buffer from main memory in lines of 32 bytes, each requiring 4 buffer cycles. In contrast to the System/370, Amdahl I/O channels as well as the CPU access the High-Speed Buffer. A tag field associated with each 32-byte line in the buffer includes a block identifier containing the high-order real address bits of the buffer data, plus parity and check fields, modification indicators, and reference bits to specify whether a central processor or channel access brought the data into the buffer and whether the CPU was in the supervisor or problem state of operation.

When a request is made for data by the central processor Instruction Unit or by the Channel Unit, the Storage Control Unit forms a pointer into the buffer and reads a 32-byte line of data from each partition of the buffer. The S-Unit then uses the real line address calculated by the address translation hardware to select one of the lines, and a tag comparison on the real address bits is used to select the data from the proper partition of the buffer. Location of the data in the buffer can be performed in two machine cycles, although overlapped buffer operations allow it to accept a request for data during each cycle. If the data is not in the buffer, a main storage request is generated and the request data is made available to the program and is also placed in the High-Speed Buffer.

Operation of the High-Speed Buffer is based on a non-store-through technique, in which data that is modified in the buffer is not written to main storage until the line is removed from the buffer to make room for new data. As a result, frequently referenced data can be accessed and modified in the buffer without incurring a large number of main memory accesses. An instruction prefetch function can be enabled for accesses to the buffer from input/output channels, the operand stream, or the instruction stream. A combination of three bits in the Storage Unit controls the order of prefetch operations, although that order can be modified through the use of an additional register bit provided for that purpose. Six operating state register bits are used to control the operation of the buffer replacement algorithm. Four additional bits of the S-Unit operating state register can be set through the System Console, can be used to partition the buffer to configure out a portion of the buffer with a hardware failure.

DYNAMIC ADDRESS TRANSLATION: The dynamic address translation facility is located in the S-Unit and controls the translation of program-specified virtual addresses into real-memory addresses. Virtual memory implementation in the 470V's is similar to that of the IBM System/370. Virtual storage is divided logically into segments of 64K bytes or 1024K bytes, which are in turn divided into pages of either 2048 or 4096 bytes. Segment and page tables are maintained in main storage to perform address mapping. A high-speed Translation Lookaside Buffer (TLB) is used to store the most recently referenced addresses, and a Segment Table Origin (STO) stack stores information on the size and main memory location of the segment table associated with TLB entries.

The 470V/5 through the 470V/6-II TLB consists of 128 virtual and real address pairs in each of the primary and alternate halves, while the 470V/7B through the 470V/8 TLB contains two halves, each with 256 address pairs.

Translation of virtual to real addresses for data located in the TLB is overlapped with the High-Speed Buffer search, and data for both real and virtual operation can be accessed in two S-Unit cycles. If the data is not located in the TLB, an address translation is performed and two additional storage references are required to locate the data either in High-Speed Buffer or in main memory. The new translated address is translated in the TLB according to an algorithm similar to that used by the High-Speed Buffer.

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virtual-storage operations comparable to those of the System/370, Amdahl has extended its design for more efficient operation. The Amdahl DAT feature maintains a segment table origin (STO) stack that allows up to 32 (128 in the 470V/7B through 470V/8) different virtual-storage environments to maintain translation information in the Translation Lookaside Buffer, reducing the amount of updating activity in the buffer.

When the capacity of the STO stack is exceeded, the oldest entry in the stack and its associated translation lookaside buffer entries are purged during spare machine cycles. In the 470V/5 and 470V/6, the translation lookaside buffer portion of the address translation hardware has also been expanded to 256 entries, compared to the System/370's 128. In the 470V/7 series and the 470V/8 the number of entries is 512.

Each I/O channel can be configured as a byte multiplexer, a block multiplexer, or a selector channel. Byte multiplexer channels have a maximum data transfer rate of 110,000 bytes per second. Block multiplexers and selectors can transfer data at 2 million bytes per second, or at 4 million bytes per second using the optional two-byte interface.

The aggregate data rate, however, is the limiting factor in each system, and this, in turn, is governed by the channel-to-processor interface circuitry of each four-channel group. The exact aggregate data rate is heavily dependent on the system configuration, but a rule-of-thumb value is available. The aggregate data rate is about 14 million bytes per second to 18 million bytes per second depending on the processor model.

A dynamic priority allocation scheme based on the availability of space in each channel buffer is used to allocate cycles between central processor operations and input/output data transfers. Normally, the central processor has the highest priority in the system, but channels performing high-speed data transfers are allowd to take precedence over the central processor by the Amdahl internal priority scheme. This allows high-speed devices to be attached to any channel without performance degradation and provides additional flexibility in the configuration of peripheral subsystems.

COMPETITIVE POSITION

Competitively, the waters were tranquil until IBM announced its Model 3033 processor. The original Amdahl 470V/6 was priced very close to IBM's 370/168 and offered about 1.5 times the performance.

The 3033 announcement caused Amdahl to adjust prices downward and started a move/counter move strategy between itself and IBM. Since the original 3033 announcement, Amdahl introduced 470V/7A with a performance factor of 1.8 x 3032. Also introduced at the same time was a 470 Accelerator which provides the 470V/7A with the same performance of 470V/7 with a simple operator

The STO stack contains virtual-storage identification fields (32 in the 470V/5 through the 470V/6-II and 128 in the 470V/7B through the 470V/8 associated with the TLB entries. The identification fields correspond with address translation information such as segment table size and location, contained in Control Register 0 and Control Register 1. When the contents of these registers are modified, subsequent TLB entries are assigned a new STO ID by the S-Unit, but earlier TLB entries are not invalidated provided they do not exceed the capacity of the stack (32 or 128). If Control Registers 0 and 1 are restored to a previous value, any previous TLB entries remaining are thus still available. The S-Unit controls selective purging (when an STO entry is automatically removed from the stack and its associated TLB entries invalidated) of the TLB and STO stack during spare cycles.

CENTRAL PROCESSOR

Central processor functions such as instruction fetching and decoding and instruction execution are performed by two separate units, the Instruction Unit (I-Unit) and the Execution Unit (E-Unit).

The I-Unit controls instruction execution through a pipeline structure and can have to six instructions concurrently in some phase of execution. The instruction execution process is divided into the fetch phase plus six additional decoding and exeuction phases. The instruction fetching operation requires three cycles, while Phases A, B, and C, which perform instruction decoding, operand address generation, and operand retrieval, each require a minimum of two central processor cycles. Phases D, E, and F each require a minimum of one cycle, and perform execution plus checking and writing of the results of the instruction execution. The overlapped instruction execution in the pipeline can result in the completion of an instruction execution every two machine cycles, except in the case of long instructions requiring additional cycles for execution.

Extensive parity checking is performed throughout the I-Unit. All incoming instructions are checked for parity, and the results are checked again after completion of execution. All control registers and the program status word are checked each time they are used. In addition, parity is checked for the timer and the address generation function, and parity is also maintained for all program-referable data.

The Execution Unit (E-Unit) executes arithmetic and logical instructions received from the I-Unit; it consists of a logical unit and checker (LUCK), a group of functional units (multiplier, adder, shifter, and byte mover), a table lookup unit to generate an inverse in the I-register (for divide operations), registers for storage of intermediate results, and a result register for output of the result of instruction execution to the I-Unit. Instruction operation codes plus control information are sent from the I-Unit to the E-Unit, and instruction operands are received either from the I-Unit or directly from main storage. The LUCK checks the validity of incoming operands, performs logical operations and comparisons on incoming operands, validates decimal digit formats, sets conditions codes, and counts leading zeroes for use in shifting and normalization. LUCK operations require one CPU cycle. Additional arithmetic functions are performed by the multiplier, adder, shifter, and byte mover units, each of which also completes its functions in one machine cycle.

When instructions require processing by multiple E-Unit functions, the I-Unit synchronizes the operation of its pipeline by delaying the progress of other instructions in the pipeline until the final cycle of the instruction that is currently in the E-Unit. The E-Unit performs parity checks on all incoming data and on logical and shift operations, and uses a check summation technique to verify the results of

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command. Amdahl has countered every IBM move in the 303X product line. The latest round occurred with IBM's announcement of Newport (3033N) in response to Amdahl's 470V/7A, and price reductions on the 303X/370 product line. Amdahl countered four days later with price reductions of its own on the whole 470 product line along with the announcement of the 470V/7B.

One aspect of the IBM 3033 that could have caused trouble for Amdahl was IBM's increased use of system-level microcoding in the 303X. This technique goes beyond the implementation of the basic instructions in microcode and adds frequently-used operating system functions to the 303X's firmware complement. By implementing portions of the operating system in firmware, IBM has made it difficult for the new MVS/SE enhancement program product for its MVS operating system to be executed in current Amdahl systems. Amdahl has responded with the development of a software solution to the problem through MVS/SE Assist.

SOFTWARE

Amdahl maintains a Software Systems Support group in Sunnyvale, California that supplies its own versions of the supported IBM Systems releases. Supported operating system software includes OS/VS1, SVS, MVS, and VM/370. Amdahl also provides support for IBM subsystems such as TSO, TCAM, JES2, JES3, VTAM, RSCS, CMS, and IPCS. Amdahl-developed software includes VM/PE, which allows a user to get increased performance from MVS or SVS when running VM/370; the previously mentioned MVS/SE Assist; and IMS/VS HDAM, designed to improve the performance of the IMS/VS data base management system. IMS/VS HDAM is the first Amdahl Internally Developed Software (AIDS) product. AIDS products are being designed to improve system performance and productivity of the DP staff, but are developed and supported by individuals and are distributed on an as is basis with no warranty.

USER REACTION

In the following chart, the ratings from 13 Amdahl users, with 18 installed systems, are shown. These ratings were extracted from the 1979 Datapro annual general-purpose computer survey. This survey was published in August 1979, and the results shown in this report were updated through a special mail questionnaire in November 1979.

Among the respondents participating in the survey, four represented educational institutes, one a minicomputer manufacturer, one an equipment manufacturer, a life insurance company, a publishing house, a railroad, and a state government department. Of the 13 users, 11 had one installed system, one had five systems, and another had two systems installed. Represented in the survey were three 470V/5's, eight 470V/6's, five 470V/6-II's, and one 470V/7. One respondent did not specify his system model designator.

addition and multiply functions. The E-Unit also generates parity for final instruction execution results, and the parity is checked by the I-Unit before storing the final results.

Failure to complete the execution of an instruction because of a hardware malfunction results in a machine check condition. Most instructions in the Amdahl 470 repertoire can be automatically retried by the E-Unit. The instruction retry feature attempts to re-execute the failed instruction (in contrast to returning the machine state to a hardware checkpoint). Instructions that cannot be retried on recovered result in a hard machine check, which is handled according to standard System/370 procedures.

Unique to the Amdahl 470's, is the "fourth-generation" LSI packaging technique that was developed to reduce both physical system size and power consumption. The basic logic unit of the 470 system is a "chip" that contains 75 to 100 emitter-coupled logic (ECL) circuits and requires significantly less power. Each chip has its own air cooling fins. The chips are mounted in multiple chip carriers that can contain up to 42 of the LSI circuits. The MCC's are, in turn, connected to a computer backplane with the chip cooling fins protruding into an air stream. The V5's and V6's contain 51 MCC, the V7's and V8's, 60 MCC. The use of air cooling in the 470V systems is a distinct advantage over the liquid cooling required by their IBM counterpart, the 370/168 and 3033.

PROCESSOR FEATURES: The standard timing features of the System/370 architecture are included in all Amdahl central processors. These include a CPU timer and a Clock Comparator; the latter provides a means for causing an interrupt when the standard Time-of-Day Clock reaches a program-specified value. Additional instructions are provided to set and store the Time-of-Day Clock, Clock Comparator, and CPU Timer.

Other features of the System/370 found in Amdahl processors include control registers, direct addressing, double word buffer, interval timer, machine check handling, multiple bus architecture, time-of-day clock, channel command retry, channel indirect addressing, byte-oriented operand feature, console audible alarm, remote console, remote data link, console file, extended control mode, and program event recording. Control registers are used for operating systems control of relocation, priority interruption, program event recording, error recovery, and masking operations. A double-word buffer consists of a 64-bit area temporarily reserved for data used in performing an I/O operation. Each channel attached to the CPU has a fixed amount of channel control buffer dedicated to its use.

The interval timer is a 32-bit decremental counter that is reduced by one several hundred times per second. The timer generates an interrupt when the contained value is decremented from a positive to a negative number. Machine check handling analyzes errors and attempts recovery by retrying the failed instruction if possible. If retry is unsuccessful, it attempts to correct the malfunction or to isolate the affected task. Multiple bus architecture implies that the various segments of the processor, namely memory, arithmetic and logic, central control, etc., are tied together by more than one central bus. The time-of-day clock is incremented once every microsecond and provides a consistent measure of elapsed time suitable for the indication of date and time. Some channels have the capability to perform channel command retry, a channel and control-unit procedure that causes a command to be retried without requiring an I/O interruption. Channel Indirect Addressing (CIA) is a companion feature to dynamic address translation, providing data addresses for I/O operations. CIA permits a single channel command word to control the transmission of data that crosses noncontiguous pages in real main storage. If CIA is not indicated, then channel one-level (direct) addressing is employed.

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The operating systems in use were OS/MVT, OS/VS1, SVS, MVS, and VM/370. OS/MVT turned out to be the most prevalent operating system in use; being installed on six systems. The users were writing applications in COBOL, FORTRAN, PL/1, and BAL. They all reported that in-house personnel were responsible for writing most of the applications software, although three users did indicate that they used a contract programming house to supplement in-house efforts and eleven specifically mentioned that all supplementary work was handled via proprietary software from independent vendors.

Seven users acquired their systems through outright purchase; two leased from the manufacturer; and four leased through a third party acquisition. Eleven users noted that their systems were acquired for business data processing primarily, three respondents said that the primary application of their systems was scientific/engineering, and one user indicated real-time control as the major use. Eight users said that they used data communications, and nine reported employing data base management systems. The average length of installation was 22 months.

Tabulated below are the ratings as submitted by the Amdahl users surveyed.

	Excellent	Good	Fair	Poor	WA*
Ease of operations	5	8	0	0	3.4
Reliability of mainframe	7	5	1	0	3.5
Maintenance service:					
Responsiveness	7	5	1	0	3.5
Effectiveness	7	5	1	0	3.5
Technical Support	2	8	1	0	3.1
Manufacturers software:					
Operating system	2	7	1	0	3.1
Ease of programming	1	10	0	0	3.1
Ease of conversion	5	7	0	0	3.4
Overall satisfaction	5	8	0	0	3.4

*Weighted Average on a scale of 4.0 for Excellent.

In general, the ratings show a strong feeling of satisfaction on the part of these users. Comments received from users were direct and to the point, and mostly complementary. Some of these comments were: "Amdahl processors are very reliable—they have the computing capacity we need. They were able to deliver and install the equipment within our time requirements. We found their FE and CE staff to be very good," "Amdahl's principle strengths are the internal speed, up-time, and ease of maintenance of their processors," "Amdahl's principle strengths are the processor's superb reliability; excellent physical facility parameters (size, power, BTU output, no chilled water); excellent field engineering support; and the 'its our problem' attitude, regardless of third-party peripherals attached," "Amdahl's strength is in its field upgradability and excellent uptime. For the last 13 months our Amdahl system uptime has been greater than 0.996!"

Conversely, there were comments relating to shortcomings. Some of these included: "Amdahl has a problem with spare parts. We have had two major outages due to lack of spare parts and Amdahl's ability to get the parts

The byte-oriented operand feature permits storage operands of most non-privileged operations to appear on any byte boundary. Instructions must appear on even byte addresses. The console audible alarm is a device activated when predetermined events occur that require operator attention or intervention for system operation. A remote console is a console attached to a system through a data link. The remote console is configured in addition to the standard console. The remote data link allows establishment of communications with a technical data center to remotely diagnose system malfunctions. The console file is the basic microprogram loading device for the system, containing a read-only file device. The media read by this device contains all the microcode for field engineering device diagnostics, basis system features, and any optional system features. The extended control mode (EC) is a mode in which all features of the System/370 computing system, including dynamic address translation, are operational. Program event recording is a hardware feature used to assist in debugging programs by detecting and recording program events.

The Direct Control Feature, as on the System/370, provides six external interrupt lines which operate independently of the normal data channels, plus the Read Direct and Write Direct instructions which provide for single-byte data transfers between an external device and main storage.

The optional Channel-to-Channel Adapter permits direct communication between an Amdahl processor and a System/370 via a standard I/O channel. It can be attached to either a selector channel or a block multiplexer channel and uses one control unit position on either channel. In an interconnection between an Amdahl 470 and a System/360 or System/370, either system can be equipped with the Channel-to-Channel Adapter, and it is required on only one of the interconnected channels.

The Two-Byte Interface, available as an option for all selector and multiplexer channels, doubles the bandwidth of the data path between the channel and the control units which support this option.

OPERATIONAL MODES: Like the System/370, the Amdahl CPU's can operate in either the Basic Control (BC) or Extended Control (EC) mode. The BC mode maintains general upward compatibility with the System/360 architecture and programming. In the EC mode, the Program Status Word (PSW) and the layout of the permanently assigned lower main storage area are altered to support Dynamic Address Translation and other new system control functions; therefore, the virtual-storage-oriented operating systems must be used.

REGISTERS: Sixteen 32-bit general registers are used for indexing, base addressing, and as accumulators. Other program-visible registers are the same as in the System/370. Machine-dependent registers contained in the 470 processors are not visible to the user and may differ from the System/370.

ADDRESSING: The same techniques as employed in the System/370 are found in the 470 processors.

INSTRUCTION REPERTOIRE: The Amdahl 470 instruction set consists of the complete System/370 Universal Instruction Set, including the five System/370 instructions for Dynamic Address Translation. Two exceptions are the Store CPU ID (STIDI) and Store Channel ID (STIDC) instructions, which differ in their operations because of architectural differences between the System/370 and the Amdahl processors. In the Amdahl units, a machine check extended logout (MCEL) is performed by the Console Processor in its own memory, whereas in the System/370 the address in main memory and size of the machine check extended logout are dependent on the central processor

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delivered to our site," "Getting documentation on SLSS and licensed products from IBM is a disadvantage to the Amdahl user. Without an IBM CPU, it seems that IBM will not handle the ordering and delivery of manuals, microfiche, etc."

The user ratings awarded Amdahl systems do not provide much of an opportunity for analysis except that the comments, in many cases, reflect a higher degree of satisfaction than the weighted average ratings. Clearly, the system performs exactly as expected, it is fully compatible with its IBM counterparts, and Amdahl has gone beyond IBM in providing reliability and maintenance aids. Further, the Amdahl users are convinced that the company has not stopped at providing good, efficient hardware, but has assembled a highly competent field support organization is sufficient numbers to insure the highest possible system availability.□

model and control register information. Since the MCEL on the 470 is made to the Console Processor, the MCEL length field stored by the STIDP instruction is all zeroes. The model number is 0470. The STIDC instruction stores zeroes for a channel model number because all Amdahl channel types are implicit in CPU type. According to Amdahl, no system or application program is likely to be affected by these model dependencies.

INSTRUCTION TIMING: The following instruction execution times, in *nanoseconds*, have been estimated by scaling performance information supplied by Amdahl for the Model 470V/6 in the absence of specific timing data for the newer models. Timings are presented for the 470V/5, 470V/6-II, and 470V/7 as representative systems.

	470V/5	470V/6-II	470V/7
Add (32-bit binary):	110	65	40
Multiply (32-bit binary):	380	228	140
Divide (32-bit binary):	2700	1625	1015
Load (32-bit binary):	110	65	40
Store (32-bit binary):	110	65	40
Add (5-digit packed decimal):	705	423	265
Compare (5-digit packed decimal):	815	488	305
Add (short floating-point):	325	195	120
Multiply (short floating-point):	435	260	165
Divide (short floating-point):	1465	878	550
Add (long floating-point):	435	260	165
Multiply (long floating-point):	1085	650	405
Divide (long floating-point):	3465	2080	1300

PHYSICAL SPECIFICATIONS: Environmental conditions for 470 processors is given in the following table.

	Operating	Nonoperating
Temperature Range	60° to 90°F	50° to 110°F
Optimum Temperature	75°F	—
Relative Humidity Range (noncondensing)	35% to 55%	8% to 80%
Optimum Relative Humidity (noncondensing)	50%	—
Wet Bulb Temperature Range	—	—
Maximum Wet Bulb Temperature	78°F	80°F
Altitude Range (feet equivalent pressure)	—	-1,000 to +10,000
Maximum Altitude (feet equivalent pressure)	+7,000	—

The Amdahl 470 processors are air cooled and require a minimum of 12.5 tons of air conditioning and 4890 cubic feet of air per minute. Minimum BTU output for a 470 processor is 79,000 BTUs per hour. Figures are generally higher depending on the processor model and amount of memory installed. Power must be available to the Amdahl 470 power distribution unit from two sources, 415 and 60 Hz. Both sources must be four wire and three phase at 208 volts.

The 470V/5 through 470V/6-II is 70 inches long, 64.5 inches high, and 30 inches wide and weighs 1,607 pounds. The processors in the upper end of the 470 line, including the 470V/7, are 72 inches long, 64.5 inches high, and 30 inches wide and weigh 1,700 pounds.

A typical configuration layout requires a 200 by 154 or 220 by 30 inch area depending on the layout (exclusive of the console). The console requires a 173 by 113 inch area.

CONSOLE INPUT/OUTPUT

The system console includes a Data General Nova 1200 minicomputer that acts as a console processor, an operator control panel, and a 3200-character CRT display and keyboard. The console processor is also equipped with a magnetic disk cartridge that is used by the console operating system and for logout and other functions, a floppy disk unit for loading diagnostic programs, and a modem to provide for remote diagnostic services.

The console has a direct interface to the central processing unit to allow access to the status of approximately 16,000 system key logic points and setting of control and data registers. The computer-to-console interface allows diagnostic tests to be performed on the central processor modules under control of the Console Processor without regard to the operating condition of the central processor, the I/O channels, or other components of the main system. The system console is also equipped with a channel interface to a selector or multiplexer channel for operation as a standard console device.

The system console operates in three modes: the maintenance mode, the hardware command mode, and the device support mode. In the device support mode, the console emulates either an IBM 3066 system console or an IBM 3215 console printer-keyboard (using the CRT display for output in place of the 3210 matrix printers), and can be connected to either a selector or block multiplexer channel. Functions that can be performed in the hardware command mode include IPL, reset operations, display and modification of the contents of registers and main storage locations, and setting of operating conditions for the system.

INPUT/OUTPUT CONTROL

Each 470 central processor includes standard input/output channels, each of which can be configured as a byte multiplexer, block multiplexer, or selector channel. Data rates are given in the table.

The aggregate I/O data transfer rate for each system is less than the total of the maximum rates of all the attached channels. Each group of four channels shares certain hardware elements, causing contentions at the interface to the CPU.

Each selector-type channel can address up to 256 input/output devices and contains a single implicit channel for addressing one device at a time at burst-mode speeds. For the 470V/5 through 470V/6-II, an additional 1024 subchannels are available for allocation to byte multiplexer and block multiplexer operations in groups of 64, 128, or 256 subchannels. For the 470V/7B through 470V/8, 2048 subchannels are available. Channels with either 64 or 128

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assigned subchannels can be configured for shared-channel operation. In channels with 64 subchannels, 4 can be shared, while those with 128 subchannels can have 8 shared subchannels. For the 470V/7 Series and 470V/8, subchannels are allocated in groups of 32, providing a total of 2048 subchannels.

In all 470 processors, input/output operations are performed under control of the Channel Unit (C-Unit), which operates independently of central processor operations. The C-Unit consists of three major functional units called the Central Interface Control Logic (CICL), the Direct Access Control Logic (DACL), and the Operation Control Logic (OCL), plus buffers and communications areas and the Remote Interface Logic which interfaces to control units for any System/360 or System/370-compatible peripheral devices.

The CICL controls the transfer and buffering of data between the Channel Buffer Store and the peripheral devices. It polls the channels every eight cycles for data transfer requests, and transfers data from the Channel Buffer Store to the Remote Interface Logic one or two bytes at a time.

The DACL controls the movement of data between the Storage Unit and the Channel Buffer Store and has a data transfer rate of one word every eight cycles. The DACL is organized as a pipeline to allow overlapping of the functions. It polls each channel every 16 cycles for service requests, concurrently transfers data in both directions between the Storage Unit and the Channel Buffer Store, and reads or stores the results of each transfer operation.

The OCL translates channel commands and coordinates channel program execution for the C-Unit.

A dynamic priority scheme controls the allocation of service to I/O channels. Channels can issue high-priority and low-priority requests for service. Each channel is assigned a 32-byte buffer area in the Channel Buffer Store. Channels with less than half a buffer area remaining are assigned high priority, while those with more than half a buffer space available are assigned low priority. The S-Unit resolves conflicts for access to the High-Speed Buffer according to its own internal priority structure, permitting high-priority channel requests to take precedence over central processor requests for access to the High-Speed Buffer. An I/O operation is always executed at a higher priority than buffer prefetch operations.

The C-Unit performs parity checks on all input and output data transfers and on data transfers to the Storage Unit. Other functions include channel indirect addressing comparable to that implemented on the System/370, and extended channel logout.

The 470V/7B through 470V/8 I/O operations are similar to those of the 470V/5 and 470V/6-II. Although they are functionally the same, there are certain differences within the DACL and CICL units.

SIMULTANEOUS OPERATIONS: The Channel Unit operates independently of central processor operations. Both can access the HSB simultaneously and independently. Also, instruction lookahead is on four levels with a maximum of six instructions in the pipeline running concurrently with instruction execution, checking, and storage of results.

HARDWARE MONITOR INTERFACE: HMI is designed for customers who wish to monitor their 470V/7B, 470V/7A, 470V/7, and 470V/8 processors, allowing users to record up to 30 categories of signals. The HMI does not record the signals, but makes them available so that they can be utilized by hardware monitors. The types of signals processed include quantity of instructions executed, processor time in active state, processor time in problem state, number of interrupts, and channel busy time. The HMI uses electronic buffering to protect the system from hardware monitor malfunctions and user errors. A set of HMI diagnostic instructions allow user access under software control.

AMDAHL DIAGNOSTIC ASSISTANCE CENTER: AMDAC, located at Amdahl headquarters and at the East Coast support center, is maintained 24 hours per day and 7 days a week by technical support specialists to solve difficult problems that cannot be resolved by field engineering on site. Via the modem in the users' 470 console, an on-line telephone hookup can be established between AMDAC and the customer system. AMDAC maintains a variety of system consoles, any of which can perform standard diagnostic tests on the users' system.

The scan circuitry can examine or reset the logic status of any one of the circuits being monitored, providing the capability to completely test and set all latches within the system. Scanning of latch points within the processing logic can occur even if the CPU is inoperative. When a failure occurs, internal logic information is displayed on the console CRT.

470/ACCELERATOR: Available for the 470V/5, 470V/5-II, 470V/7B; and 470V/7A, the 470/Accelerator is a hardware product initiated via software commands. The 470/Accelerator is designed for users who want the option of increasing processing power upon demand without having expensive idle capacity over the long term. Performance of the 470V/5 can be increased about 40 to 50 percent to that of the 470V/6, while the 470V/5-II can be brought up to the level of the 470V/6-II. The 470/Accelerator increases performance of the 470V/7A by 15 to 25 percent, making it equivalent to the 470V/7. The 470/Accelerator becomes operational through a single operator console command. Accelerator usage is determined by a meter, activated when the processor is in accelerator mode.

PERIPHERAL EQUIPMENT

The Amdahl 470 systems can utilize all IBM System/360 and System/370 input/output and mass storage devices, as well as their plug-compatible counterparts from independent vendors. Detailed coverage of many of these peripherals can be found in Volume 2 of DATAPRO 70.

SOFTWARE

Amdahl offers complete functional compatibility with IBM 360/370/303X software. Amdahl Corporation intends to support users of current IBM system software by providing new releases of the software to Amdahl users, including minor modifications to account for differences in the way the 470's handle machine check conditions, and by supplying software support services for its customers. Modifications are analogous to installing different models of the operating system on System/370 processors. Operating systems supported include OS/MVT, OS/VS1, SVS, MVS, and VM/370. The 470 series supports OS/VS1 and SVS only on systems of eight megabytes or less. Support is included for such major IBM subsystems as HASP, ASP, TSO, TCAM, JES2, JES3, VTAM, RSCS, CMS, and IPCS. Amdahl also states that they have assisted customers in modifications to the recovery management system for system control programs including TSS, ACP, MTS, and VP/CSS.

VIRTUAL MACHINE/PERFORMANCE ENHANCEMENT (VM/PE): This software product enables an Amdahl user to run the IBM MVS or SVS control program on the same computer as the IBM VM/370 control program. Amdahl claims that the utilization of VM/PE offers significant and immediate performance improvements to the user. These improvements, according to Amdahl, could mean that users will experience MVS production operating system

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(P/OS) throughput with VM/370 that could be 94 to 97 percent of the MVS native-state throughput. The percentages are based on a 12-megabyte 470V/7 with dedicated MVS channels and no other virtual machine activity.

VM/PE implements a new dispatching interface, P/OS handling of its dedicated channel I/O operations, a restart facility for VM/370 after a control program termination without disturbing the P/OS virtual machine executive within VM/PE, and more accurate P/OS CPU time accounting. VM/PE provides increased P/OS performance by eliminating the management of shadow page tables, most privileged instruction simulation, and VM/370 control program handling of P/OS virtual machine I/O operations. VM/PE masks I/O interrupts for P/OS dedicated channels while VM/370 is in control. VM/PE Release 2.0 adds support of dedicated channel I/O masking to reduce control changes between the P/OS and VM/370. Release 2.0 also provides improved logic to reduce page zero swap overhead and a new function for the VM/370.

INDICATE command. This new function allows display on the system console of performance, timing, and load balancing information including the time interval since the last display, page zero swaps per second during the interval, P/OS-dedicated SIOs per second during the interval, VM/PE elapsed time, VM/PE total CPU usage, VM/PE CPU usage and total virtual CPU usage. VM/PE Release 2.1 adds performance measurement aids. VM/PE provides support for the following software product releases:

	VM/PE	VM/PE	VM/PE
Product & Release	1.2	2.0	2.1
VM/370 Release:	5	5 or 6	6
PLC	11 or 12	12 or 3	3
VM/BSE Release:	1.1	1.1 or 2.0	2.0
VM/SE Release:	1.0	1.0	2.0
MVS	3.7	3.7 or 3.8	3.7 or 3.8
MVS/SE	1.0	1.0	1.0 or 2.0
MVS/SEA	1.0	1.0	1.0
SVS	—	1.7	1.7

MVS/SE ASSIST: This software package is designed to emulate the microcoded MVS enhancements IBM provided in its 303X processors. MVS/SE Assist operates on all 470 processors without modifications to CPU hardware or the MVS/SE code and requires about 1500 bytes of main memory. Benchmarks performed by Amdahl on an eight megabyte 470V/6-II with MVS Release 3.7 plus MVS/SE and RMF-II indicate a 13 percent drop in supervisor state execution and a 12 percent improvement in throughput with MVS trace on. With trace off, throughput gained by 10 percent and supervisor state execution time dropped off by 11 percent.

MVS/SE Assist is activated upon execution of a System/370 extended instruction by the 470. This is done by installing an MVS/SE Assist routine to precede the program check first-level interrupt handler. This routine intercepts the operation exception program check so that the program check PSW can be analyzed to determine the type of operation requested. MVS/SE Assist normally replaces the interrupted instruction with a branch to an appropriate routine for simulation of the proper microcode.

AMDAHL INTERNALLY DEVELOPED SOFTWARE (AIDS) is a class of software designed to improve system performance and productivity of the DP staff. Software is developed for the AIDS program by Amdahl employees as software solutions to particular customer problems crop up. All AIDS programs must meet the established criteria of improving performance and or productivity, and must meet Amdahl standards for maintenance, ease of installation, and quality of documentation and coding. The program's author or representative remains responsible for product support for one year after announced program availability. AIDS products are provided "as is" without warranty either expressed or implied.

IMS/VS HDAM OPTIMIZER. The IMS/VS HDAM Optimizer is the first AIDS software released by Amdahl. It was designed to improve performance when using IMS/VS HDAM data bases. The IMS/VS HDAM Optimizer determines the optimal placement of data during normal data base reorganization, thus reducing the number of physical I/O operations necessary to process a HDAM data base. Amdahl estimates that the number of I/O requests is reduced by 10 to 15 percent. The Optimizer supports all presently existing IMS/VS options and requires no source code modifications to any presently existing IMS/VS routines, user routines, or control blocks.

In addition, the Optimizer quantitatively measures the effectiveness of various HDAM configurations. The analysis includes the randomizer, root addressable area size, and the number of root anchor points. From the analysis, the Optimizer selects the configuration with the lowest I/O estimate. IMS/VS HDAM Optimizer operates under OS/VS1, SVS, and MVS with IMS/VS releases 1.1.1 through 1.1.5.

PRICING

The Amdahl 470 systems are offered for purchase or for lease under two- or four-year operating lease plans. Leases may be renewed for 12-month periods. Lease payments must be made monthly in advance. Lease payments include the lessee charge, property taxes, and insurance, but not maintenance charges. The minimum lease term for a system upgrade is 12 months. Leases can be terminated after two years upon payment of 30 percent of the total remaining rental payments. A 90-day written notice is required for cancellation. For users wishing to purchase leased equipment, purchase credits of 50 percent of each monthly payment are allowed to a maximum aggregate credit of 50 percent of the purchase price. The purchase credit applies either to the original leasee or the current leasee.

Monthly maintenance charges are not included in lease charges. Maintenance is provided for 24 hours per day and 7 days per week.

Amdahl maintains a Software Systems Support (SSS) group in Sunnyvale, California that supplies its own versions of the supported IBM systems releases to Amdahl users. The SSS group also issues Amdahl corrections to the IBM Program Temporary Fix (PTF) tapes.

The Field Support center (FSC), also located in Sunnyvale, California, helps insure a smooth transition at installation time. The FSC also is chartered to analyze and correct problems in supported operating systems.■

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EQUIPMENT PRICES

		Purchase Price	Monthly Maint.*	2-Year Lease**	4-Year Lease**
PROCESSORS AND MAIN MEMORY					
470V/5	CPU Complex; includes 16K-byte buffer storage, console with maintenance processor, and power distribution unit; main memory and channels as indicated below.				
	With 4,194,304 bytes of main memory and:				
	8 channels	$1,472,000	$ 8,500	$ 42,300	$ 34,000
	12 channels	1,622,000	9,000	48,000	39,200
	16 channels	1,772,000	9,500	53,700	44,400
	With 6,291,456 bytes of main memory and:				
	8 channels	1,572,000	9,450	47,150	38,400
	12 channels	1,722,000	9,950	52,850	43,600
	16 channels	1,872,000	10,450	58,550	48,800
	With 8,388,608 bytes of main memory and:				
	8 channels	1,672,000	10,400	52,000	42,800
	12 channels	1,822,000	10,900	57,700	48,000
	16 channels	1,972,000	11,400	63,400	53,200
470V/5-II	CPU Complex; includes 32K-byte buffer storage, console with maintenance processor and power distribution unit; main memory and channels as indicated below.				
	With 4,194,304 bytes of main memory and:				
	8 channels	1,572,000	8,600	45,200	36,400
	12 channels	1,722,000	9,100	50,900	41,600
	16 channels	1,872,000	9,600	56,600	46,800
	With 6,291,456 bytes of main memory and:				
	8 channels	1,672,000	9,550	50,050	40,800
	12 channels	1,822,000	10,050	55,750	46,000
	16 channels	1,972,000	10,550	61,450	51,200
	With 8,388,608 bytes of main memory and:				
	8 channels	1,772,000	10,500	54,900	45,200
	12 channels	1,922,000	11,000	60,600	50,400
	16 channels	2,072,000	11,500	66,300	55,600
A70V/6	CPU Complex; includes 16K-byte buffer storage, console with maintenance processor, and power distribution unit; main memory and channels as indicated below.				
	With 4,194,304 bytes of main memory and:				
	8 channels	1,702,000	8,750	48,970	39,550
	12 channels	1,852,000	9,250	54,670	44,750
	16 channels	2,002,000	9,750	60,370	49,950
	With 6,291,456 bytes of main memory and:				
	8 channels	1,802,000	9,700	53,820	43,950
	12 channels	1,952,000	10,200	59,520	49,150
	16 channels	2,102,000	10,700	65,220	54,350
	With 8,388,608 bytes of main memory and:				
	8 channels	1,902,000	10,650	58,670	48,350
	12 channels	2,052,000	11,150	64,370	53,550
	16 channels	2,202,000	11,650	70,070	58,750
A70V/6-II	CPU Complex; includes 32K-byte buffer storage, console with maintenance processor, and power distribution unit; main memory and channels as indicated below.				
	With 4,194,304 bytes of main memory and:				
	8 channels	1,802,000	8,850	51,870	41,950
	12 channels	1,952,000	9,350	57,570	47,150
	16 channels	2,102,000	9,850	63,270	52,350
	With 6,291,456 bytes of main memory and:				
	8 channels	1,902,000	9,800	56,720	46,350
	12 channels	2,052,000	10,300	62,420	51,550
	16 channels	2,202,000	10,800	68,120	56,750
	With 8,388,608 bytes of main memory and:				
	8 channels	2,002,000	10,750	61,570	50,750
	12 channels	2,152,000	11,250	67,270	55,950
	16 channels	2,302,000	11,750	72,970	61,150
A70V/7B	CPU Complex; includes 32K-byte buffer storage, console with maintenance processor, and power distribution unit; main memory and channels as indicated below.				
	With 4,194,304 bytes of main memory and:				
	8 channels	1,450,000	8,800	58,125	46,500
	12 channels	1,600,000	9,300	65,250	52,200
	16 channels	1,750,000	9,800	72,375	57,900

*Includes 24 hours, 7 days per week on-call service.
**Charges do not include maintenance for the V/5, and V/5-II, V/6, and V/6-II models.

Amdahl 470 Systems

EQUIPMENT PRICES

		Purchase Price	Monthly Maint.*	2-Year Lease**	4-Year Lease**
PROCESSORS AND MAIN MEMORY (Continued)					
	With 8,388,608 bytes of main memory and:				
	8 channels	1,650,000	10,700	71,475	57,200
	12 channels	1,800,000	11,200	78,600	62,900
	16 channels	1,950,000	11,700	85,725	68,600
470V/7A	CPU Complex; includes 32K-byte buffer storage, console with maintenance processor, and power distribution unit; main memory and channels as indicated below.				
	With 4,194,304 bytes of main memory and:				
	8 channels	1,750,000	9,000	63,450	50,750
	12 channels	1,900,000	9,500	70,575	56,450
	16 channels	2,050,000	10,000	77,700	62,150
	With 8,388,608 bytes of main memory and:				
	8 channels	1,950,000	10,900	76,800	61,450
	12 channels	2,100,000	11,400	83,925	67,150
	16 channels	2,250,000	11,900	91,050	72,850
	With 12,582,912 bytes of main memory and:				
	8 channels	2,150,000	12,800	90,150	72,150
	12 channels	2,300,000	13,300	97,275	77,850
	16 channels	2,450,000	13,800	104,400	83,550
	With 16,777,216 bytes of main memory and:				
	8 channels	2,350,000	14,700	103,500	82,850
	12 channels	2,500,000	15,200	110,625	88,550
	16 channels	2,650,000	15,700	117,750	94,250
A70V/7	CPU Complex; includes 32K-byte buffer storage, console with maintenance processor, and power distribution unit; main memory and channels as indicated below.				
	With 4,194,304 bytes of main memory and:				
	12 channels	2,350,000	9,600	77,200	61,750
	16 channels	2,500,000	10,100	84,325	67,450
	With 8,388,608 bytes of main memory and:				
	12 channels	2,550,000	11,500	90,550	72,450
	16 channels	2,700,000	12,000	97,675	78,150
	With 12,582,912 bytes of main memory and:				
	12 channels	2,750,000	13,400	103,900	83,150
	16 channels	2,900,000	13,900	111,025	88,850
	With 16,777,216 bytes of main memory and:				
	12 channels	2,950,000	15,300	117,250	93,850
	16 channels	3,100,000	15,800	124,375	99,550
A70V/8	CPU Complex; includes 64K-byte buffer storage console with maintenance processor, and power distribution unit; main memory and channels as indicated below.				
	With 4,194,304 bytes of main memory and:				
	12 channels	2,550,000	10,050	83,750	67,000
	16 channels	2,700,000	10,550	90,875	72,700
	With 8,388,608 bytes of main memory and:				
	12 channels	2,750,000	11,950	97,100	77,700
	16 channels	2,900,000	12,450	104,225	83,400
	With 12,582,912 bytes of main memory and:				
	12 channels	2,950,000	13,850	110,450	88,400
	16 channels	3,100,000	14,350	117,575	94,100
	With 16,777,216 bytes of main memory and:				
	12 channels	3,150,000	15,750	123,800	99,100
	16 channels	3,300,000	16,250	130,925	104,800
MEMORY					
	2-Megabyte Memory Increment for 470V/5, 470V/5-II, 470V/6, and 470V/6-II	100,000	950	5,450	4,950
	4-Megabyte Memory Increment for 470V/7 Series and 470V/8	200,000	1,900	14,700	11,800

*Includes 24 hours, 7 days per week on-call service.
**Charges do not include maintenance for the V/5, and V/5-II, V/6, and V/6-II models.

Amdahl 470 Systems

EQUIPMENT PRICES

	Purchase Price	Monthly Maint.*	2-Year Lease**	4-Year Lease**
PROCESSOR OPTIONS AND UPGRADES				
Channel to Channel Adapter for all processors	32,500	—	1,000	900
Two-Byte Interface for all processors	1,400	—	50	40
Field Upgrade 470V/5 to 470V/5-II	125,000	100	3,200	2,650
470V/6 to 470V/6-II	125,000	100	3,200	2,650
470V/5 to 470V/6	330,000	250	7,350	7,000
470V/5-II to 470V/6-II	330,000	250	7,350	7,000
470V/5 to 470V/6-II	455,000	350	10,400	9,550
470V/7B to 470V/7A	325,000	200	5,900	4,675
470V/7A to 470V/7	475,000	100	7,300	5,850
470V/7 to 470V/8	250,000	450	7,200	5,775
Four Channel Group for 470	175,000	500	6,300	5,800
Four Channel Group for	175,000	500	7,850	6,275
Hardware Monitor Interface for 470V/7B through 470V/8	40,000	150	1,865	1,400

*Includes 24 hours, 7 days per week on-call service.
**Charges do not include maintenance for the V/5, and V/5-II, V/6, and V/6-II models.

SOFTWARE PRICES

LEASE OR LICENSE ONLY PRODUCTS

	Monthly Lease Fee	Monthly License Fee	Comments
VM/Performance Enhancement			
Release 2.0	—	$1,500	per installed system
Release 2.1	—	1,500	per installed system
470/Accelerator Hardware	$1,800	—	for 20 meter hours plus $90 for each additional hour
MVS/SE Assist	—	250	per installed system
Amdahl Internally Developed Software (AIDS) IMS/VS HDAM	—	225	per installed system for 24 months