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Apple Macintosh / 3.5-Inch Sony Microfloppy Disk

Interface Design Document

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19 May 1983

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Contents:

Note: this is a revision of the 2 May Sony Interface Design Document. This version extends the descriptions of /MOTORON and /STEP (pages 2 and 3), and adds two new sections: Motor Speeds (page 4) and Hardware Interface (page 11).

INTRODUCTION

This document describes the mechanical, electrical, and software interface between an Apple Macintosh computer and a Sony 80 track, 3.5 inch microfloppy disk drive.

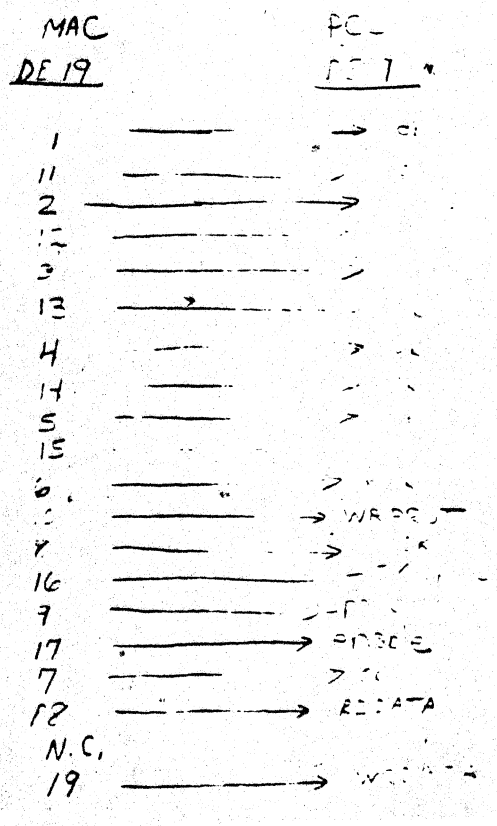
The interface supports auto-eject operation, allowing the disk cassette to be ejected from the machine under software control. In addition, a connector signal (/PWM) allows the speed of the drive motor to be adjusted under software control, which increases the drive capacity and keeps the speed of the media, with respect to the head, relatively constant. For future versions which may use two read-write heads, (allowing data to be recorded on both sides of the disk), a control signal (SEL) is provided at the connector.

Apple intends to use the drive with a proprietary GCR (Group Code Recording) encoding scheme. This scheme reads and writes code words containing 2, 4, or 6 microsecond intervals between flux transitions.

PINOUT FOR APPLE MACINTOSH DISK INTERFACE CONNECTOR

This table shows the signal names associated with the pins of an Apple Macintosh 20-pin disk drive connector.

Signal Name	Connector Pin No.
CGND	1
CA0	2
CGND	3
CA1	4
CGND	5
CA2	6
CGND	7
LSTRB	8
-12VF	9
/WRTGATE	10
+5VF	11
SEL	12
+12VF	13
/ENBL	14
+12VF	15
RD	16
+12VF	17
WRTDATA	18
+12VF	19
/PWM	20



MCI CONTROL INPUTS, OUTPUTS, AND STATUS BITS

Note: the control signals and status bits described here refer to the Microfloppy Control Interface IC (MCI) installed on the disk drive's Read-Chain board. An "input" refers to one of the MCI inputs, likewise for the outputs.

There are four control inputs to the MCI:

Ø. /CSTIN This input goes to a zero only when a cassette is in the drive.

1. WRTPRT This input goes to a one only when a write-protected cassette is in the drive, or when no cassette is in the drive.

2. TKØ This input goes to a one only when the head is located at track Ø. From the time the /STEP output is brought low, a delay of 12 mS is required before the TKØ input is valid.

3. TACH This input receives 6Ø pulses for each rotation of the drive motor. The signal is used for accurate calibration of motor speed.

Note: when these inputs are read on the RD line, as described in the following section, all of the signals except /CSTIN appear inverted.

There are four control outputs from the MCI:

Ø. /DIRTN This output sets the direction of head motion for stepping from one track to another. A zero sets the direction towards the center of the disk. When the drive is disabled (/ENBL high), the /DIRTN output is set to a one.

1. /STEP If the drive is enabled (/ENBL low), setting the /STEP output to a zero tells the disk's CPU to begin a full track step sequence. When the step sequence is complete (within 12 mS), the disk's CPU sets the /STEP output to a one. When the drive is disabled (/ENBL high), the /STEP output is set to a one.

2. /MOTORON If the drive is enabled (/ENBL low) and a cassette is in the drive (/CSTIN low), setting the /MOTORON output to a zero turns on the drive motor. From the time /MOTORON is brought low, a delay of 400 mS is required before valid read data may be expected from the drive. When the drive is disabled (/ENBL high), /MOTORON cannot be changed.

3. EJECT If the drive is enabled (/ENBL low), setting the EJECT output to a one causes the cassette to be ejected from the drive. When the drive is disabled (/ENBL high), the EJECT output is set to a zero.

There are two readable status bits coded internally in the MCI:

6. SIDES This status bit is read as a zero if the drive is single-sided (one read/write head), or a one if the drive is double-sided.

7. /DRVIN This status bit is read as a zero only if the selected drive is actually connected to the Apple Macintosh computer.

READING AND WRITING ON THE MCI

To read an MCI control signal or status bit, or the RDDATA signal from a disk read/write head, first be sure that LSTRB is low and the drive is enabled (/ENBL low). Then follow the chart below to determine the correct state of CAØ, CA1, CA2 and SEL for the desired signal. This signal will then appear on the RD line. Note that all of the MCI input signals except /CSTIN are inverted when they appear on the RD line.

CA2	CA1	CAØ	SEL=Ø	SEL=1
Ø	Ø	Ø	/DIRTN	/CSTIN
Ø	Ø	1	/STEP	/WRPROT
Ø	1	Ø	/MOTORON	/TKØ
Ø	1	1	EJECT (Write only)	/TACH
1	Ø	Ø	RDDATA (Head Ø)	RDDATA (Head 1)
1	1	Ø	SIDES	SIDES
1	1	1	/DRVIN	/DRVIN

The state of all the signals except EJECT can be read. However, you can write to only four signals: the control outputs /DIRTN, /STEP, /MOTORON and EJECT. To write to one of the control outputs , begin by following the instructions for reading the signal, as above, but set CA2 to the value (Ø or 1) to which you wish to set the control output. Next, bring LSTRB first high and then low.

Note 1: be sure that CAØ-CA2 and SEL do not change value while LSTRB is high, and that CAØ and CA1 are returned to a one level before changing SEL.

Note 2: EJECT is an unlatched output only: the state of the EJECT signal cannot be read (it always reads the value Ø). To eject a cassette, follow the instructions for setting the EJECT output to a 1, but hold LSTRB high for approximately one-half second.

Note 3: the MCI output /MOTORON will not actually affect the drive unless a cassette is in the drive.

Note 4: after you set /STEP to a Ø, the disk drive resets it to a 1 within 12 mS. However, you must always set LSTRB low before the disk resets /STEP to a 1. To be safe, make sure that LSTRB is high less than 1 mS except during eject.

/PWM SIGNAL CHARACTERISTICS

The /PWM signal is used by the computer to adjust the speed of the drive motor. This TTL level signal transmits timing information in the form of pulses whose average width width determines the motor speed. The basic pulse rate is 22 kHz, and the duty cycle of each pulse (the portion of time the signal is at a logic zero level) may vary from Ø% to 9Ø%. However, the signal is dithered such that ten pulses must be averaged to reconstruct the true motor speed, giving an effective frequency of 2.2 kHz.

MOTOR SPEEDS

The following table shows the correct motor speed for each of the 8Ø disk tracks:

Track	Speed (rpm)
Ø....9	363
1Ø...25	393
26...4Ø	429
41...55	472
56...71	524
72...79	59Ø

MCI PAL EQUATIONS

```
PAL16L8              BURRELL SMITH & GEORGE CROW
PAT0010              2-MAY-83
MICROFLOPPY CONTROL INTERFACE (MCI)

CA0 CA1 CA2 LSTRB /ENBL SEL RDDATA /CSTIN WRTPRT GND
TK0 EJECT LE /DIRTN /STEP 05 /MOTORON TACH RD VCC

LE = /LSTRB * /SEL +

     /CA2 * /CA1 * /CA0 * CSTIN * SEL +

     /CA2 * /CA1 * CA0 * WRTPRT * SEL +

     /CA2 * CA1 * /CA0 * TK0 * SEL +

     /CA2 * CA1 * CA0 * TACH * SEL


/DIRTN = /CA2 * /CA1 * /CA0 * LE * /SEL +

         DIRTN * SEL +

         DIRTN * CA1 +

         DIRTN * CA0 +

         DIRTN * /LSTRB +

         /ENBL


/STEP = ENBL * 05 * /CA2 * /CA1 * CA0 * LE * /SEL +

        ENBL * 05 * STEP * SEL +

        ENBL * 05 * STEP * CA1 +

        ENBL * 05 * STEP * /CA0 +

        ENBL * 05 * STEP * /LSTRB


/MOTORON = ENBL * /CA2 * CA1 * /CA0 * LE * /SEL +

           MOTORON * SEL +

           MOTORON * /CA1 +

           MOTORON * CA0 +

           MOTORON * /LSTRB
```

```
EJECT = /CA2 * CA1 * CAØ * LSTRB * /SEL +
        SEL +
        /CA1 +
        /CAØ +
        /LSTRB +
        /ENBL

IF (ENBL) RD = /CA2 * SEL * /LE +
               /CA2 * /CA1 * /CAØ * /SEL * DIRTN +
               /CA2 * /CA1 * CAØ * /SEL * STEP +
               /CA2 * CA1 * /CAØ * /SEL * MOTORON +
               CA2 * /CA1 * /CAØ * /RDDATA +
               CA2 * CA1 * CAØ +
               CA2 * CA1 * /CAØ  /
```

DESCRIPTION:

THIS PART INTERFACES THE 3.5-INCH SONY DISK TO MACINTOSH.

NOTE: THIS IS PATTERN (REVISION) NUMBER 1Ø. THIS PART'S CHECKSUM IS: ØF5Ø .

FUSE PLOT OF MCI PAL DEVICE

Microfloppy Control Interface (MCI Pattern 10)

	0123	4567	8911 01	1111 2345	1111 6789	2222 0123	2222 4567	2233 8901
0	----	----	----	-X--	----	----	----	----
1	----	-X--	----	----	X---	----	---X	----
2	-X-X	-X--	----	----	-X--	---X	----	----
3	-XX-	-X--	----	----	-X-X	----	----	----
4	X--X	-X--	---X	----	-X--	----	----	----
5	-X-X	X---	----	----	----	-X--	----	----
6	X-X-	X---	----	----	----	----	----	----
7	X--X	X---	----	----	----	----	----	----
8	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
9	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
10	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
11	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
12	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
13	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
14	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
15	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
16	----	----	----	----	----	----	----	----
17	X--X	-X--	----	-X--	-X--	----	--X-	----
18	----	----	---X	----	X---	----	----	----
19	-X--	----	---X	----	----	----	----	----
20	--X-	----	---X	----	----	----	----	----
21	----	----	-X-X	----	----	----	----	----
22	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
23	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
24	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
25	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
26	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
27	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
28	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
29	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
30	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
31	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX

	Ø123	4567	89ıı ØI	1111 2345	1111 6789	2222 Ø123	2222 4567	2233 89Ø1
32	----	----	----	----	----	----	----	----
33	-XX-	-X--	----	-XX-	-X--	----	--X-	----
34	----	----	----	-XX-	X--X	----	----	----
35	X---	----	----	-XX-	---X	----	----	----
36	---X	----	----	-XX-	---X	----	----	----
37	----	----	-X--	-XX-	---X	----	----	----
38	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
39	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
4Ø	----	----	----	----	----	----	----	----
41	-X-X	-X--	----	----	-X--	----	--X-	----
42	----	----	----	----	X---	---X	----	----
43	X---	----	----	----	----	---X	----	----
44	--X-	----	----	----	----	---X	----	----
45	----	----	-X--	----	----	---X	----	----
46	----	----	----	X---	----	----	----	----
47	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
48	----	----	----	----	----	----	----	----
49	----	----	-X--	----	-X--	----	----	----
5Ø	-X-X	-X--	----	----	X---	----	-X--	----
51	-XX-	-X--	----	----	X---	----	----	X---
52	X--X	-X--	----	----	X---	----	----	--X-
53	X-X-	-XX-	----	----	X---	----	----	----
54	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
55	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX
56	----	----	----	----	----	----	----	----
57	X-X-	-X--	X---	----	-X--	----	----	----
58	----	----	----	----	X---	----	----	----
59	-X--	----	----	----	----	----	----	----
6Ø	---X	----	----	----	----	----	----	----
61	----	----	-X--	----	----	----	----	----
62	----	----	----	X---	----	----	----	----
63	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX	XXXX

Legend: X = Fuse Not Blown (L,N,Ø)
\- = Fuse Blown (H,P,1)

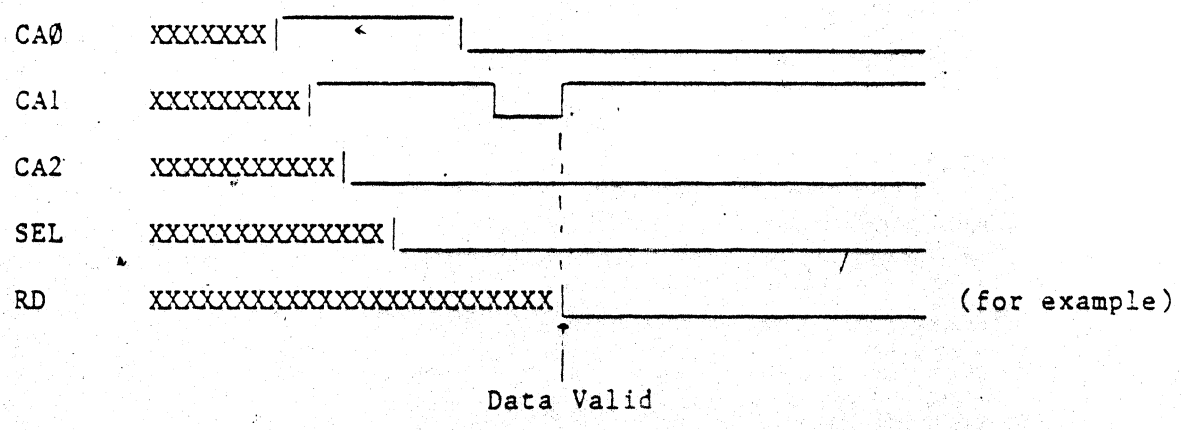
Number of Fuses Blown = 1168

MCI TIMING DIAGRAMS

Unless indicated otherwise, timing is variable, but must not be less than 1 µS between transitions. In these diagrams, XXXX indicates a period when the signal is in an unknown state (either high or low, or floating).

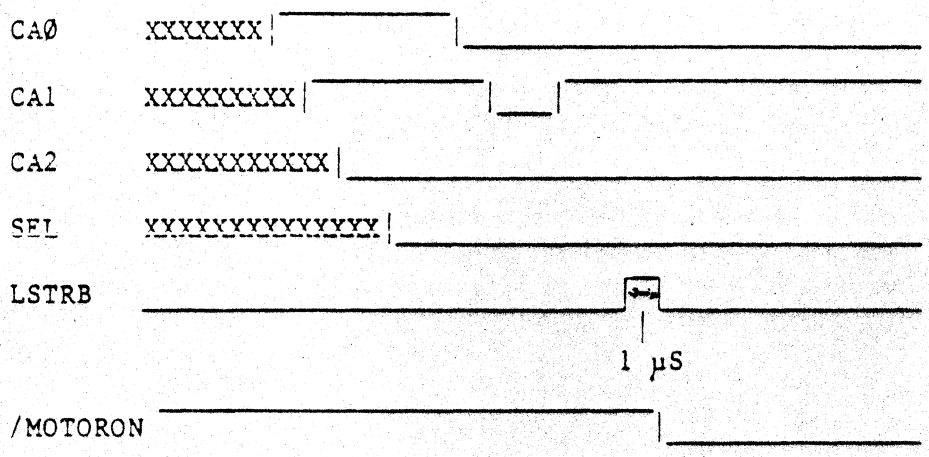
1. Read MCI Control Line

This example reads the state of the /MOTORON line. The equation for doing this is: CAØ=Ø, CA1=1, CA2=Ø, SEL=Ø . (Note: CA1 goes low before returning to a one for the convenience of software, only.)



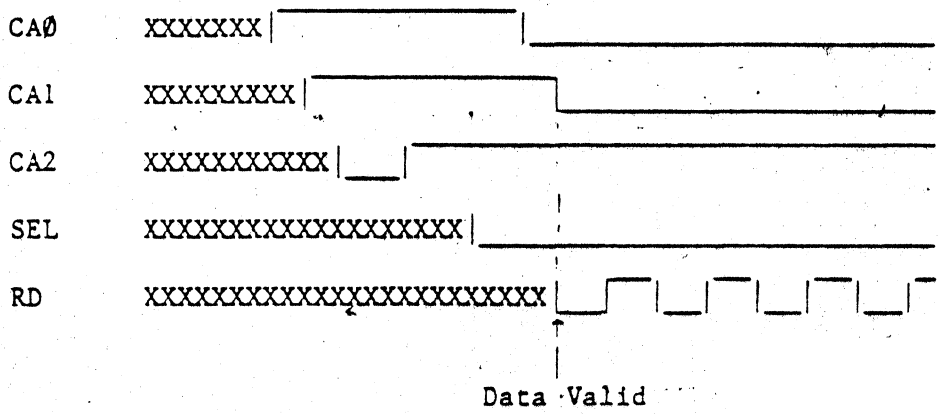
2. Write to MCI Output Line

This example changes the state of the /MOTORON line from high to low. (Note: CA1 goes low before returning to a one for the convenience of software, only.)

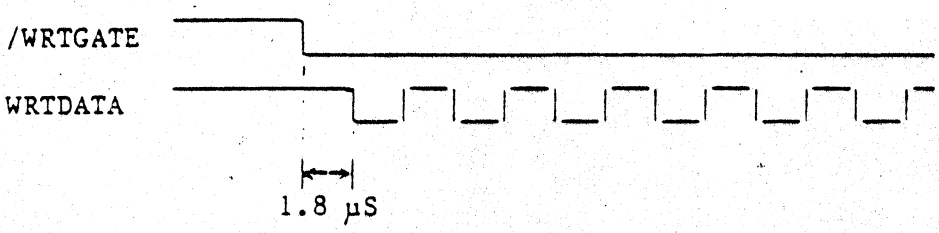


3. Read Data

This example reads data from disk read/write head Ø . On a single-sided drive, correct data will be read no matter which head is selected. (Note: CA2 goes low before returning to a one for the convenience of software, only.)



4. Write Data



Note: After a write, the minimum time before reading is 100 µS.
After a read, the minimum time before writing is 1.8 µS.

HARDWARE INTERFACE

The following table shows the input and output characteristics of the Sony hardware interface.

Power Supply Requirements:

Voltage Required	Current Required
+12 V, +-5%	Ø.4 A
+ 5 V, +-5%	Ø.5 A
-12 V (Note 1)	Not used

Outputs:

Signal Name	Output Current IOH	Output Current IOL	Output Voltage VOH	Output Voltage VOL
RD (Note 2)	-1 mA	6.5 mA	2.4 V	Ø.5 V

Inputs:

Signal Name	Input Current IIH	Input Current IIL	Input Voltage VIH	Input Voltage VIL
/WRTGATE, WRTDATA (Note 2)	-Ø.9 mA	-1.5 mA	2.Ø V	Ø.8 V
CAØ-CA2, LSTRB, SEL	25 µA	-Ø.25 mA	2.Ø V	Ø.8 V
/ENBL	125 µA	-Ø.75 mA	2.2 V	Ø.8 V
/PWM	1Ø µA	-4Ø µA	2.Ø V	Ø.8 V

Note 1: -12 V is available at the disk drive connector, but -12 V is not used by the Sony drive.

Note 2: The RD and WRTDATA signal lines include a 3.3K pull-up resistor to +5 volts.

Note 3: When reading data from the disk, the RD output will put out a positive-going pulse of approximately 5ØØ nS duration for each flux transistion actually recorded on the disk. During the write operation, however, each transistion of the WRTDATA line whether positive-going or negative-going will cause a flux transistion to be written on the disk.