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	MICROPROCESSOR POT/PIN INTERFACE	MPPI/S-16

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ABSTRACT and CONTENTS

This document describes the hardware, programming conventions, and timing of the standard microprocessor Pot/Pin interface.

This document describes the hardware, programming conventions, and timing of the standard microprocessor pot-pin interface.

A. The Hardware

The pot-pin interface is implemented on a single 136 pin printed circuit card. The interface card contains drivers and receivers for the following signals:

1) 24 bits of output data from the Z register.
2) 24 bits of input data to the E2 bus.
3) Attention latches 1,2,and 3 inputs to the microprocessor branch logic.
4) ALERT, POT, and PIN, and TUCLR outputs from the microprocessor special function card.
5) The global clock, which may be regenerated and used by external devices.
6) +5 VOLTS

SN74H40N IC's are used for both drivers and receivers. The receiver inputs are terminated to +5V through 270 ohm. All busses connected to external devices are 'low true.' The drivers and receivers are assumed capable of operating with up to 12 T^2L loads in addition to the loading introduced by interconnecting cables. The inputs of the E2 receivers are sources of approximately 20 m.a. each, making them compatible with SN74H010N, SN74H05N, and SN74H22N open collector gates. Using a worst case figure of 100 p.f. per line, and 12 wire-or gates connected to the bus, the charging time for the E2 line is 36 nsec.

The physical arrangement of the interface card and busses is as follows:

The interface card will occupy a slot approximately six spaces from the end of the microprocessor card cage. The remaining five slots are reserved for I/O devices which are built on 136 pin p.c. cards. The interface card itself will be pin compatible with the AMC-TSU cable card, and in the AMC, will be replaced by the cable card. Thus in the AMC, the TSU's are the only device which can be connected to the I/O system. At the edge of the cage, the I/O busses will be connected to 2 amphenol 221 series connectors. These connectors will be used to connect external devices such as the CHIO multiplexer via twisted pair cables. In the event no external devices are connected, a dummy plug will be inserted which will have 360 ohms resistors to ground and +5V terminating the Z', ALERT', POT', PIN', and CLOCK' lines. The E2' lines and ATTENTION' will be left open. This scheme implies that no device inserted into the final 5 slots of the rack should terminate the outbound lines. In the event external devices are connected, the outbound lines should be terminated to ground and +5V with 360 ohms at the end of their cables.

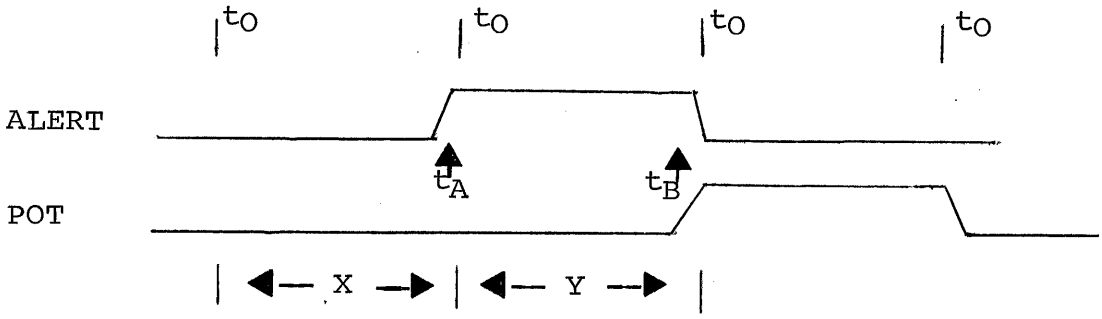
B. Timing and Programming

The normal instruction sequence for doing output to a device is to execute:

DEVICE ADDRESS —▶ Z, ALERT;

DATA —▶ Z, POT;

This instruction sequence results in the following signal sequence:

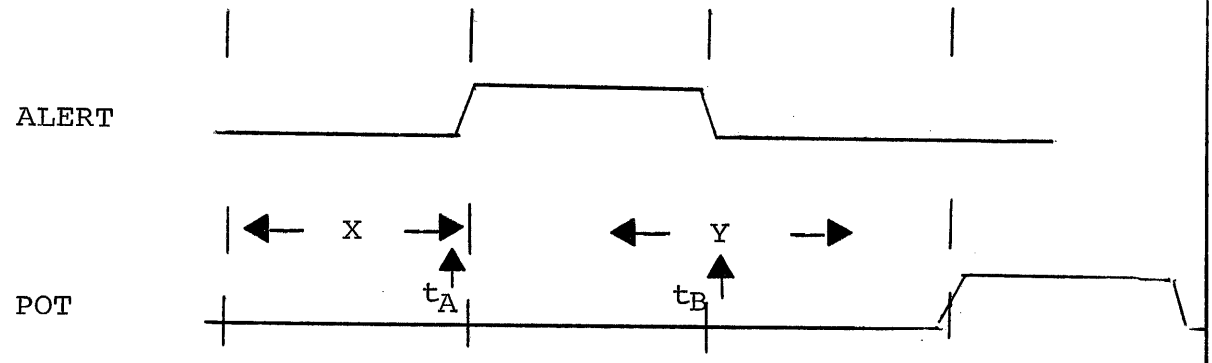


t_O is the 'system reference time'. It is approximately coincident with the fall of K2 at the microprocessor. The first instruction above is executed during the interval designated 'X'. The second is executed during 'Y'. The Z register is loaded with the device address at t_A, and with the output data at t_B. If the external device requires more than 1ØØ nsec to set up the data path, or if the external register is loaded with the POT strobe (rather than POT.K2), the following sequence may be executed:

D.A —▶ Z, ALERT;

DATA —▶ Z, VCY, POT;

The resulting signal sequence is:



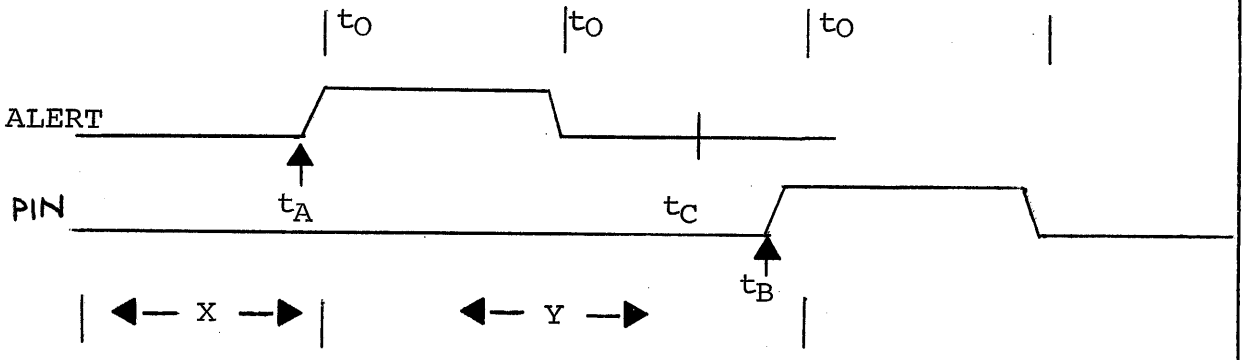
The general rule on timing of the ALERT, POT, and PIN strobes is that they rise at the end of the instruction* during which the special condition is executed, and they fall at the end of the first interval* during which the special condition does not exist. Thus it is possible to generate arbitrarily long strobes, but this should be avoided.

The <u>normal</u> sequence for doing input from a device is to execute:

DEVICE ADDRESS --▶ Z , ALERT

PIN; TE2Y, VCY; or PIN, TE2Y, UNCONDITIONAL BRANCH;

The resulting signal sequence is:



* An instruction may be more than 1 interval long.

The first instruction is executed during the interval 'X', the second during 'Y.' The device address is loaded into Z at t_A, and the microprocessor loads the data into one of its internal registers at t_B. The external device must have the data stable on the E2 bus no later than $t_C = t_O + 42$ nsec.

If this timing is not usable due to limitations in the external device, the following sequence may be used:

DEVICE ADDRESS ⟶ Z, ALERT;

NOP or NOP, VCY;

PIN, TE2Y;

This allows an extra 1ØØ or 2ØØ nsec. between the presentation of the device address and the utilization of the returned data.

The Bryant TSU's require a different POT/PIN sequence than most other I/O devices. The restriction on the TSU's is that output data will remain stable on the Z bus for 200 nsec before ALERT or POT falls, and that input data will be allowed 200ns to stabilize before the fall of PIN. The instructions required to obtain this sequence are:

1) OUTPUT

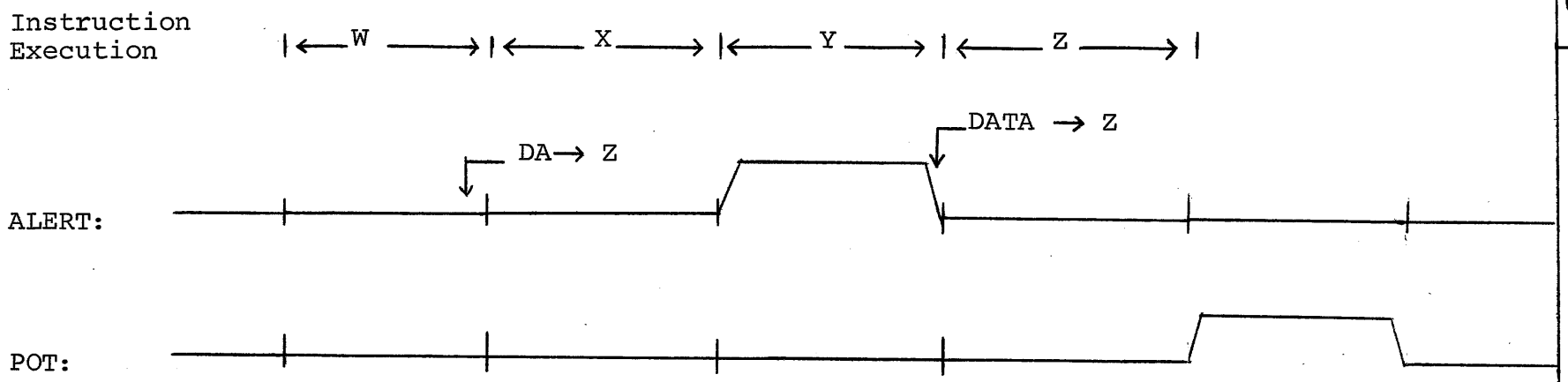
W: D.A ⟶ Z;

X: ALERT;

Y: DATA ⟶ Z;

Z: POT;

Which results in:



2) INPUT

W: D.A. → Z;

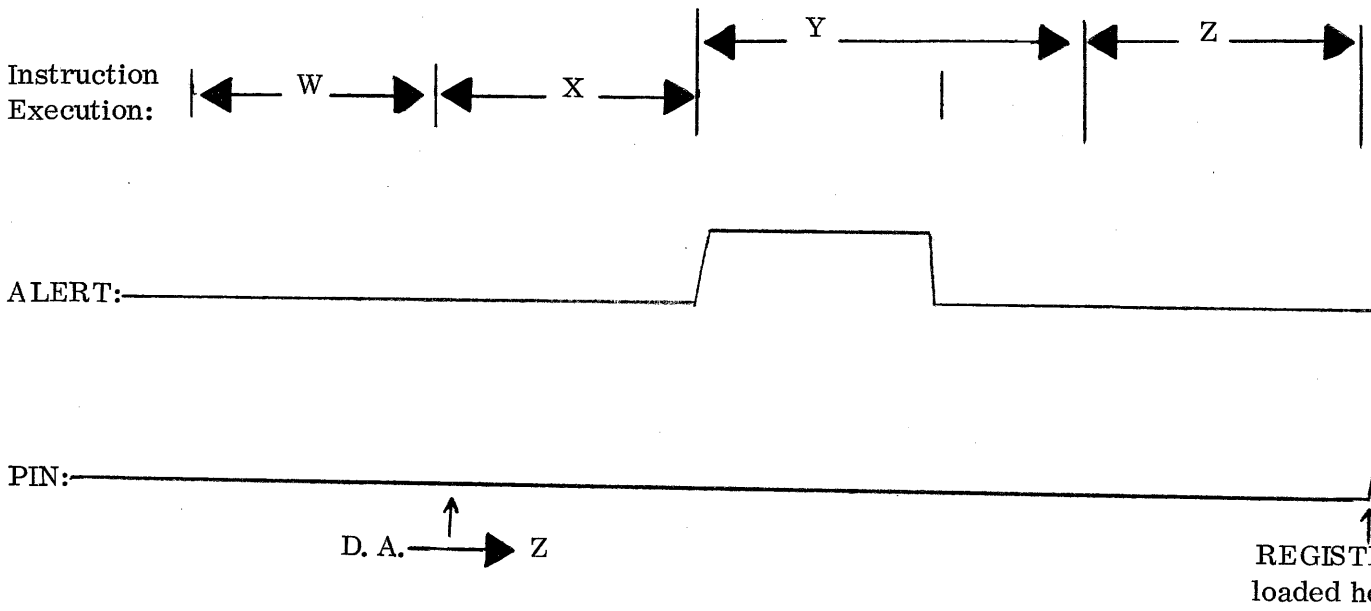
X: ALERT;

Y: VCY, NOP

Z: TE2Y, Y → REGISTER; PIN

Which results in:

W: DA



The ATTENTION' signals are requests for service generated by external devices. These signals set latches in the microprocessor which may be tested and reset by branch conditions.

Ideally, ATTENTION' is a 100 nsec pulse overlapping t_0.

The branch tests on the attention latches cause a branch on the latch not set. The latch is reset during the interval in which the branch test is done (STATE A if VCY=Ø, STATE B if VCY = 1) unless the external device is attempting to simultaneously set the latch, in which case it is set. Attention latch #1 also has a test for the latch set, but the reset conditions are the same as described above. The specification for a particular device should be consulted to determine the attention latch to which it is connected (if any), as well as the correct POT/PIN sequence to use.

The signal TUCLR is a d.c. reset signal used by the TSU (and possibly by other devices). It is set by the special condition RESET T.U. Unlike POT, PIN, and ALERT, it exists during the instruction in which the special condition is set, rather than the interval after the execution of the instruction. This is possible since the effects of TUCLR on the external device are assumed to be time-independent.