bcc	title: INTEGRAL TEST PROCESSOR REFERENCE MANUAL	prefix/class-number.revision: ITPRM/W-23

checked: L. Peter Deutsch	authors	approval date: 9/11/69	revision date:
checked: Jack Goldman	Butler W. Lampson	classification: Working Paper	
approved: Mef	Butler W Lampson	distribution: Company Private	pages: 13

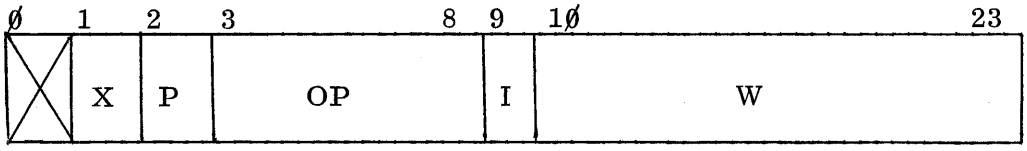
ABSTRACT and CONTENTS

The instruction set of the integral test processor (ITP) in the M1 microscheduler is described. The relationships between the ITP and the rest of the world are described in ITPEX/W-22, which should be read in conjunction with this document.

Table of Contents

Introduction

The ITP is an approximate subset of the SDS 930. It is a 24-bit, twos complement machine. An instruction has the format



X = indexing

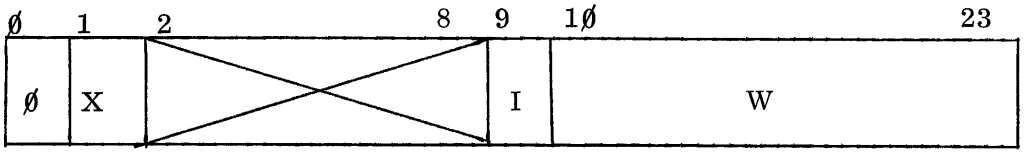
P = pop bit

OP = opcode

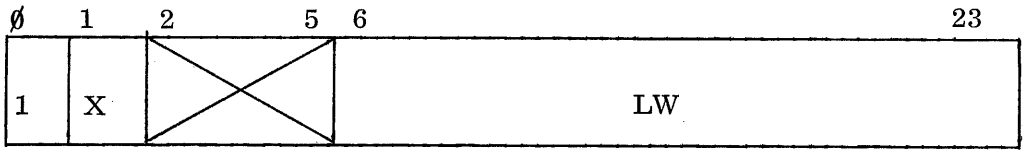
I = indirection

W = word address

There are two formats for an indirect word. A normal IAW is



An absolute IAW is



LW = long word address

There are three 24-bit central registers called A, B, and X, a 14-bit program counter P, memory relocation and bounds registers REL and BOUND, and I/O control register IOCTL and a mode register MODE. The last four are discussed in ITPEX.

Addressing

All instructions compute the effective address of the instruction word I in the same way:

```
        T  ← I;
LOOP:   Q  ← W(T);
        Q  ← W(Q+XR)  IF X(T);
        IF I(T) DO;
            T  ← CONTENTS(Q);
            GOTO LOOP IF T > = ∅;

* ABSOLUTE INDIRECTION
            Q  ← T;
            Q  ← Q + XR IF X(T);
            Q  ← LW(Q) + 4B7;
        ENDIF;
```

The function CONTENTS returns the contents of the memory location addressed by its value.

All memory references in ITP, with the exception of references using an effective address which was obtained by absolute indirection, are called

relative and are made in the following way.

If Q is the address, location

Q + REL

in the M1 central memory is referenced, where REL is the memory relocation register. Furthermore, if the reference is for a store, there is a trap unless

Q < BOUND

where BOUND is the memory bound register. Note that a relative address cannot be greater than 37777B.

If Q is an absolute address, then location Q in the memory is referenced and there is no store protection. All specific addresses mentioned in the manual are relative; an absolute address can be generated only by indirection through an absolute IAW. An absolute address will be interpreted as relative if it appears in a branch or EAX instruction. I. e., BRU* = 4ØØØØØ1ØB will send control to relative location 1ØB.

When the machine is reset (see below), REL and BOUND are set from two absolute locations in the M1 core. They may be altered by the program at any time.

Instructions

All instructions, and the values of OP for each, are listed in Appendix I, together with the sub-cases of the SHIFT, RCH and UPS instructions.

All machine instructions have P = Ø. Instruction words with P = 1 are pops

and are discussed in the next section.

This section describes all the instructions, categorized by general function. The symbols, AR, BR, XR, P stand for the registers, Q for the effective address, D for CONTENTS(Q). T is a temporary. The function STORE(V) stores V in the memory location addressed by Q. STORE (V, L) stores V in location L.

Every instruction ends with P ← P + 1 unless it sets P explicitly or executes the parameterless function SKIP. In the latter case it ends with P ← P + 2.

Data Transfer:

LDA:	AR ← D;
LDB:	BR ← D;
LDX:	XR ← D;
STA:	STORE(AR);
STB:	STORE(BR);
STX:	STORE(XR);
XMA:	T ← D; STORE(AR); AR ← T;

Arithmetic:

ADD:	AR ← AR + D;
SUB:	AR ← AR - D;
MIN:	STORE (D + 1);
ADM:	STORE (D + AR);

Logical:

ETR: AR ← AR AND D;

MRG: AR ← AR OR D;

EOR: AR ← AR EOR D;

Skip:

SKE: SKIP IF AR = D;

SKM: SKIP IF AR AND B = D AND B;

SKG: SKIP IF AR > D;

SKA: SKIP IF AR AND D = ∅;

SKB: SKIP IF BR AND D = ∅;

SKN: SKIP IF D < ∅;

SKR: STORE (D-1); SKIP IF D - 1 < ∅;

Branch:

BRU: P ← Q;

BRX: XR ← XR + 1; P ← Q IF XR AND 40000B ≠ ∅;

BRM: STORE (P); P ← Q + 1;

BRR: P ← D + 1;

Shift:

The action of the SHIFT instruction is determined by bits 13 - 15 of Q. If this field is >4, the instruction traps. The A and B registers are shifted as a single 48-bit register, by an amount C given by bits 18 - 23 of Q, as follows:

LCY	left cycle
LSH	left shift, bring in ∅
RSH	right shift, bring in sign of A
LRSH	right shift, bring in ∅
RCY	right cycle

Register Change:

The action of the RCH instruction is determined by bits 12 - 15 of Q, as follows. Here CR is a control register determined by bits 22 - 23.

XCA:	T ← AR; AR ← CR; CR ← T;
CCA:	AR ← CR;
CLAB:	AR ← BR ← ∅;
CLA:	AR ← ∅;
CLB:	BR ← ∅;
CLX:	XR ← ∅;
CAB:	BR ← AR;
CBA:	AR ← BR;
XAB:	T ← AR; AR ← BR; BR ← T;
CBX:	XR ← BR;
CXB:	BR ← XR;
XXB:	T ← XR; XR ← BR; BR ← T;
CXA:	AR ← XR;
CAX:	XR ← AR;

XXA: T ← XR; XR ← AR; AR ← T;

CNA: AR ← -AR;

Miscellaneous:

NOP: no action

EXU: execute D as an instruction word

EAX: XR ← (Q AND 37777B) OR (XR AND 7774B4);

HLT: trap

Input/Output:

UPOT: outputs BR to the device addressed by AR

UPIN: inputs to BR from the device addressed by AR

The I/O instructions are discussed in detail in ITPEX/W-22.

Communication with other microprocessors:

The UPS instruction decodes bits 14 - 15 of Q to select an operation. If a parameter is required, bits 16 - 23 of Q are used.

STR: strobes the microprocessors selected by the operand

PRO: sets the protects selected by the operand, turns off the microscheduler and saves the state of schedule mode in bit 3 of MODE.

UPR: clears all protects and restores schedule mode from bit 3 of MODE.

Pops

If P = 1, the instruction is a pop, and executes as follows:

STORE (P OR 40000B, Ø);

P ← 100B + OP;

Trap

A trap or reset can occur if

an illegal instruction is executed

the store protection is violated

the ITP is started by instruction to the US.

A trap reloads REL and BOUND from fixed absolute core locations, clears IOCTL, stores P in 2, and sends control to 3.

940 Compatibility

The instruction and indirect word formats are the same, except that the sign bit of an indirect word is interpreted. The opcodes are different.

The MUL, DIV, ADC, SUC, NOD, SKD and overflow test instructions are absent, as are all I/O instructions.

The RCH instruction is completely different.

The SHIFT instruction has a different format. Its address is computed like all other instructions. The shift is done Mod 64 instead of Max 48.

There is no overflow bit. Hence, BRM does not save it, and BRR does not restore it. Also, bits 1 - 8 of the word stored by BRM and pops are zero.

X 0′ is not affected by arithmetic operations.

The sign bit of a pop is ignored.

APPENDIX I: ITP Instructions

ØØ	HLT	26	MIN
Ø1	BRU	27	XMA
Ø2	ETR	3Ø	ADM
Ø3	MRG	31	SHIFT
Ø4	EOR	32	SKM
Ø5	NOP	33	LDX
Ø6	EXU	34	SKA
Ø7	STA	35	SKG
1Ø	STB	36	LDB
11	STX	37	LDA
12	BRX	4Ø	EAX
13	BRM	41	UPS
14	UPOT		
15	UPIN		
16	RCH		
17	SKE		
2Ø	BRR		
21	SKB		
22	SKN		
23	SUB		
24	ADD		
25	SKR		

APPENDIX I: continued

SHIFT, bits 13 - 15 of Q

ø	LCY
1	LSH
2	RSH
3	LRSH
4	RCY

RCH, bits 12 - 15 of Q

ø	XCA	16	XXA
1	CCA	17	CNA
2	CLAB		
3	CLA		
4	CLB		
5	CLX		
6	CAB		
7	CBA		
1ø	XAB		
11	CBX		
12	CXB		
13	XXB		
14	CXA		
15	CAX		

APPENDIX I: continued

Control Register for XCA, CCA, bits 22 - 23 of Q

ø	MODE
1	REL
2	IOCTL
3	BOUND

UPS, bits 14 - 15 of Q

ø	STR
1	UPR
2	PRO
3	Undefined