MOSTEK MDX-FLP2

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Preface

This manual serves as a reference to Mostek's MDX-FLP2, a floppy disk controller for the STD-Z80 bus. MDX-FLP2 can control both single density, single sided and double density, double sided Shugart compatible disk drives. In addition, MDX-FLP2 can control up to four 8 inch or up to three 5 1/4 inch disk drives.

The manual is divided into three sections. The first section serves as an introduction to FLP2. A general overview of FLP2 is presented. In addition, the features and specifications of FLP2 are briefly discussed.

Section two serves as the User's Guide to FLP2. This section describes how to install FLP2 in the user's system. Included is a discussion of minimum system requirements, strapping options and disk connection suggestions. Also included are procedures for insuring that FLP2 is properly installed.

Section three is the OEM (Original Equipment Manufactures) Guide. This section includes information useful to programmers interested in using FLP2 in custom applications. This section includes a discussion of both the MK3883 DMA Controller and the WD1797 Floppy Disk Controller. The section ends with a discussion of the hardware design of FLP2.

The Appendices contain useful reference information. This includes a schematic and a parts list. Also included is a listing of the STD-Z80 Bus signals used by FLP2.

1. INTRODUCTION TO MDX-FLP2

MDX-FLP2 is a floppy disk drive controller board for the STD-Z80 bus. The MDX-FLP2 board embodies all required controlling, formating and interface logic between the STD-Z80 bus and one to four floppy disk drives. Used with Mostek's M/OS-80,' a CP/M compatible disk operating system (available separately), FLP2 transforms any STD-Z80 bus system into a versatile, floppy disk based computer system.

FLP2 can control both single-density, single-sided and double-density, double-sided Shugart compatible disk drives. In addition, either 5 1/4 or 8 inch drives may be used. Transfers to and from the disk are normally handled by the powerful MK3883 DMA Controller; programmed data transfer is also possible. Multiple FLP2 boards can be operated simultaneously since daisy chained priority DMA operation is possible.

FLP2 operates with a wide variety of disk drives. Included are drives by Shugart Associates and Remex. Either 5 1/4 or 8 inch drives may be used; simply change three straps to convert FLP2 from a 5 1/4 inch controller to an 8 inch controller. Write precompensation is also strapable.

Since FLP2 is based on the WD1797 Floppy Controller, many advanced features are available. These include IBM 3740 or IBM System 34 diskette formatting capability, automatic track seek with verification, programmable step rate, and automatic CRC generation and checking. In addition, single sector, multi-sector, or complete track transfers are possible.

1.1. SUMMARY OF MDX-FLP2 FEATURES

- STD-Z80 Bus Compatible
- Controls Single and Double Density Disk Drives
- Controls Single and Double Sided Disk Drives
- Controls up to four 8 inch drives; up to three 5 1/4 drives
- Jumper selectable to handle either 5 1/4 or 8 inch drives
- Up to 4 Mhz operation
- Provision for priority DMA daisy chain operation
- Provision for external devices to use DMA Controller
- Jumper selectable port addresses in blocks of eight
- Jumper selectable in main port space or IOEXP space
- Jumper selectable write precompensation
- Soft sector operation, including variable-length sectors
- IBM 3740 and System 34 diskette formatting capability
- Automatic track seek with verification
- Programmable step rate
- DMA or programmed data transfer
- Interrupt driven or polled operation
- Automatic CRC generation and checking
- Single sector, multi sector or full track data transfers
- Compatible with Mostek's M/OS-80 and FLP80 (using FLP2-DCF)

1.2. SPECIFICATIONS

1.2.1. Electrical Specifications

Data Bus: 8 bits, bidirectional

Address Bus: 16 bits, lower 8 bidirectional, upper 8 output during DMA activity

System Bus: STD-Z80 Compatible

Inputs: One 74 LS Load Max

Outputs: I_{OH} = 15 mA min at 2.5 V

I_{OL} = 24 mA min at 0.5 V

System Clock: Up to 4 Mhz

I/O Addressing: 8 ports on board selectable to any of 32 eight port slots by jumper options; board may be placed in main I/O space or expansion I/O space (IOEXP)

Memory Addressing: On board DMA capable of addressing any memory address (Note: MDX-CPU1 does not allow external addressing of its scratch pad memory)

Power Requirements: +12V $\pm$ 5% @ 100mA max
+5V $\pm$ 5% @ 1.2A max

Operating Temperature: 0°C to 60°C

1.2.2. Mechanical Specifications

Card Dimensions

4.5 in (11.43 cm) high by 6.50 in (16.51 cm) long

0.48 in (1.22 cm) maximum profile thickness

0.062 in (.16 cm) printed circuit board thickness

Connectors

STD-Z80 Bus (J1) - 56 pins with .125 in. center

Drive Interconnect (J3) - 50 pins with .100 in. center

DMA Daisy Chain (J2) - 8 pin dual right angle, .1 in center

Mating Connector for STD Bus (J1)

P.C. 3VH28/1CE5 (Viking)

Soldertail 3VH28/1CN5 (Viking)

W.W. 3VH28/1CND5 (Viking)

Mating Connector for Drive Interconnect (J3)

609-5000 W/O Strain Relief (Ansley)

609-5001 with Strain Relief (Ansley)

Mating Connector for DMA Daisy Chain (J2)

1-86148-8 (AMP)

2. INSTALLATION GUIDE

This section describes a step-by-step procedure for installing the MDX-FLP2 board. In addition, a procedure for connecting a floppy disk drive to the FLP2 board is given.

2.1. MINIMUM SYSTEM HARDWARE REQUIREMENTS

The minimum system requirements vary depending on the intended application of FLP2. However, the procedures discussed in this manual assume the following minimum system:

- A serial ASCII terminal, i.e., TTY, Silent 700 or CRT
- MDX-CPU, MDX-UART, MDX-RAM (system dependent) and MDX-FLP2
- A 5 1/4 or 8 inch floppy disk drive and media
- Power Supplies for the above equipment

2.2. Unpacking

No special unpacking procedures are necessary. However, if the shipping package is damaged, notify the carrier. If the package is in good condition, carefully open and remove the MDX-FLP2 board.

CAUTION: Some of the integrated circuits in this assembly are high impedance MOS devices. Internal circuitry is included on each device to protect the inputs against damage due to static voltage; however,leave the assembly in the conductive bag until ready for installation.

2.3. OVERVIEW

Figure 2-1 shows a block diagram of a typical system using FLP2. The FLP2 board plugs into any STD-Z80 bus. A cable connects FLP2 to the disk drive(s). In addition, an appropriate power supply for both the STD-Z80 boards and the floppy disk is required.

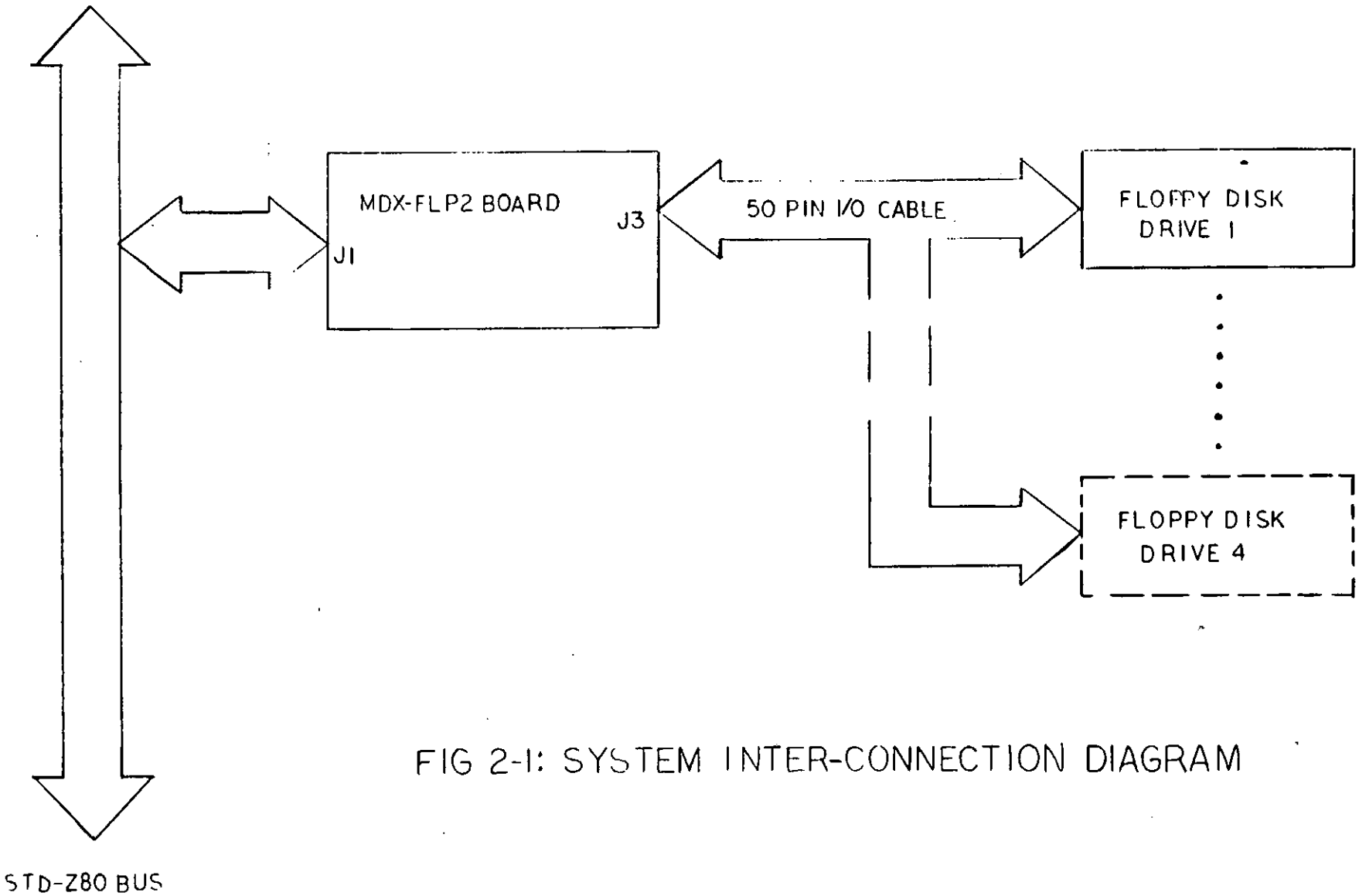


FIG 2-1: SYSTEM INTER-CONNECTION DIAGRAM

2.4. STRAPPING OPTIONS

FLP2 is a versatile board since the user may customize the board to varying tasks by changing straps. Figure 2-2 shows the locations of the strapping locations, J4-J12. The following discussion explains the purpose of each strap, and how the strap is set from the factory.

NOTE: If the user's system contains 8 inch drives and uses Mostek's MOS/80 or FLP80 DOS, this section may be skipped -- the strapping options are factory set for such systems.

J4: Auto Precomp - When open, double density write precompensation is always in affect (provided DDEN* is low). This is primarily for 5 1/4 inch drives that require write precompensation on every track. When strapped, write data is precompensated only for tracks greater than 43; this is the factory setting.

J5: Test Points - Test points shown on the schematic are located on this jumper.

J6: VCO Clock - This clock is either a 4 Mhz clock (pins 1 and 2 strapped) for 8 inch drives or a 2Mhz clock (pins 3 and 4) for 5 inch drives.

J7: 8 inch Ready - When using an 8 inch drive, this strap connects the Ready signal to FLP2. When using a 5 1/4 inch drive, this strap is not connected. Thus, 5 1/4 inch drives will always appear ready.

J8: 8 or 5 1/4 inch Clock - Strap for either a 4 Mhz clock (pins 3 and 4) for 8 inch drives or a 2 Mhz clock (pins 1 and 2) for 5 inch drives.

J9: 5 1/4 inch drive - This strap is used by Mostek software to determine whether 5 1/4 or 8 inch drives are used. Only strap J9 for 5 1/4 inch drives.

J10: Port Address Select - This options allows the user to place FLP2 on any of 32 possible 8-port boundaries. Figure 2-3 shows the various straps. Note that a jumper installed implies a logic zero. The factory setting is E0H (11100XXX).

J11: I/O Expand - IOEXP* is normally not used on Mostek boards. Thus, the factory straps pins 2 and 3. If the user desires to use IOEXP*, strap pins 1 and 2; also strap pins 3 and 4.

J12: EXT Ready Level - This jumper determines whether the EXT RDY input to the FLP2 DMA is active low or active high. For an active high EXT RDY, strap pins 1 and 2; for an active low EXT RDY, strap pins 2 and 3 (factory setting).

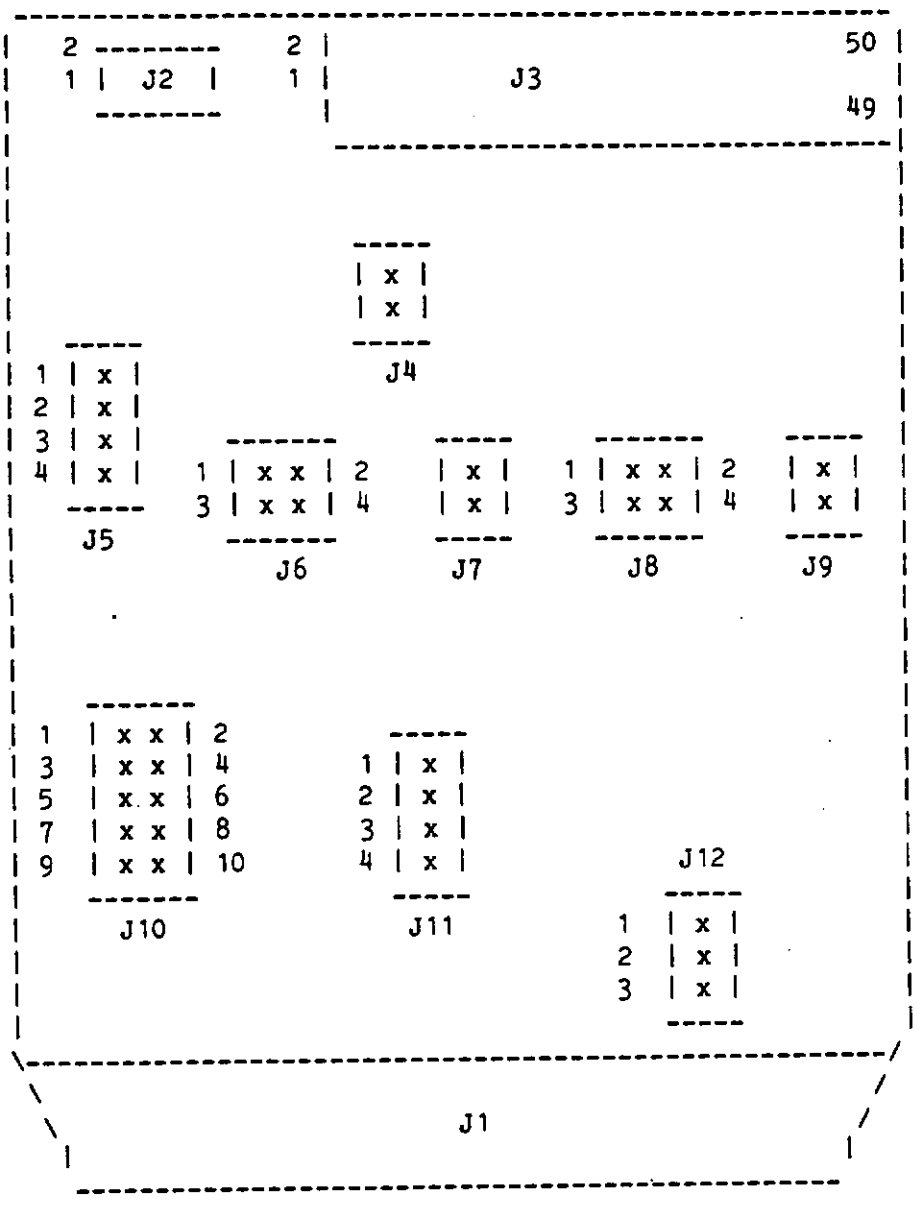


Fig. 2-2: FLP2 Strapping Locations

Address	Corresponding Pins on J10	Factory Setting
A7	10 and 9	not strapped (1)
A6	8 and 7	not strapped (1)
A5	6 and 5	not strapped (1)
A4	4 and 3	strapped (0)
A3	2 and 1	strapped (0)

NOTE: A strap installed implies a logic zero.

Fig. 2-3: Address Strapping Options

2.5. DMA DAISY-CHAIN OPTION

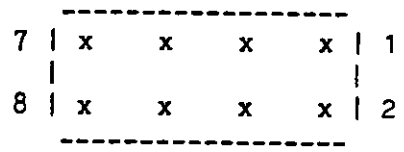
The MDX-FLP2 is designed to allow the option of multiple DMA boards in the same system. The two signals -- BAI (Bus Acknowledge In) and BAO (Bus Acknowledge Out) -- which create the priority DMA daisy chain are implemented by connecting the signals to J2, an 8-pin connector at the top of the board. In addition, pin 8 of J2 may be used for external devices -- for example a PIO or SIO -- to access the READY pin of the MK3883 Controller.

The configuration of the connector is shown in Figure 2-4. Twisted pair cables with two-contact connectors at each end are used to connect the bus priority chain.

2.5.1. DMA Daisy Chain Operation

As shown in Figure 2-4 and Figure 2-5, the daisy chain is implemented using J2, an eight pin 0.025" square post header. Bus Acknowledge In (BAI) is on pin 2, while Bus Acknowledge Out (BAO) is on pin 4.

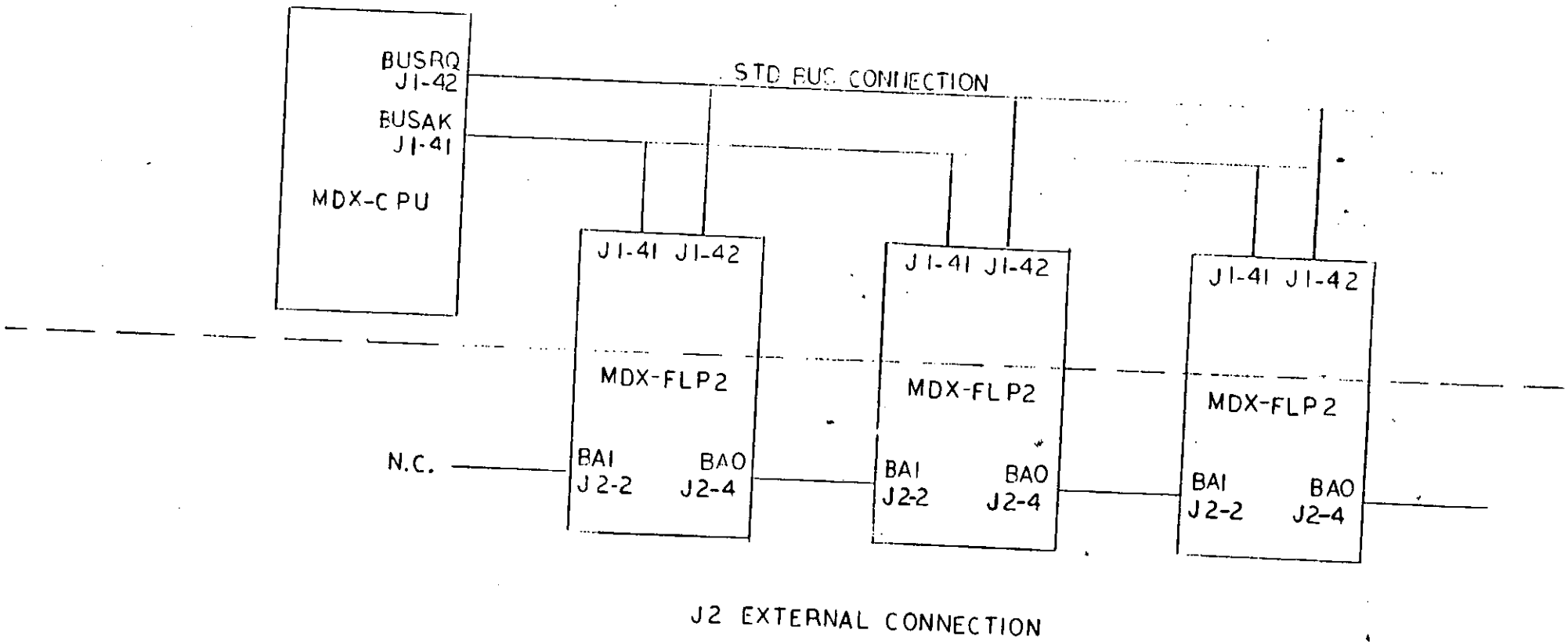
Suppose a system requires the use of two FLP2 boards. As shown in Figure 2-5, the highest priority FLP2 is DMA device 1, while the lower priority FLP2 is DMA device 2. Thus, the FLP2 cards are prioritized for multiple DMA operation.



J2 - Top View

Pin No.	Function
1,3,5,7	Ground
2	BAI (Bus ACK In)
4	BAO (Bus ACK Out)
6	No connection
8	External DMA Request Input

Fig. 2-4: DMA Daisy Chain Connector



J2 EXTERNAL CONNECTION

HIGHEST PRIORITY 2nd-HIGHEST PRIORITY 3rd-HIGHEST PRIORITY····ETC.

NOTE: EACH MDX-FLP2 CONTROLLER MUST BE STRAPPED FOR DIFFERERENT I/O ADDRESS

FIG. 2-5: MDX-FLP2 MULTIPLE DMA BUS PRIORITY CONNECTIONS

2.6. INSTALLATION INTO STD-Z80 BUS

At this point, FLP2 may be installed for initial check-out. With the system power off, place FLP2 into an empty card slot.

CAUTION: Installing FLP2 with the power on may result in a nonworking board.

Once FLP2 is installed in a card slot, power up the system.

2.7. MDX-FLP2 CHECKOUT

Communication between the MDX-CPU1, MDX-UART, and MDX-FLP2 is assured by executing the following tests. Note that it is not necessary to have a disk connected to FLP2 at this point. Also, note that Mostek's DDT Monitor is used. The following conventions are used:

1. (CR) indicates a Carriage Return

2. ^ indicates a Carat or Up Arrow

3. ___ underline indicates portion of command entered by the user.

Use the following examples to verify correct operation of FLP2.

1. Test for communication between DDT and FLP2.

```
.P   E3(CR)
E3   XX  FF^    ;write FF to port 3 (drive select)
E3   FF  00^    ;read port 3, write port 3
E3   F0  .      ;exit
```

2. Check FLP2 status.

```
.P E2 (CR)      ;read status port 2
E2   XX .       ;where XX is one of the following:

     BC = Single sided, no interrupt, 8 inch drive
     BD = Double sided, no interrupt, 8 inch drive
     BE = Single sided, interrupt, 8 inch drive
     BF = Double sided, interrupt, 8 inch drive
     9C = Single sided, no interrupt, 5 1/4 inch drive
     9D = Double sided, no interrupt, 5 1/4 inch drive
     9E = Single sided, interrupt, 5 1/4 inch drive
     9F = Double sided, interrupt, 5 1/4 inch drive
```

Note that the above conditions are normal indications after a master reset condition.

3. Check Track, Sector and Data Register.

```
.P   E5(CR)      ;port 5, track register
E5 XX  FF^       ;write to track register
E5 FF  00^       ;verify write, clear track register
E5 00  .         ;verify clear and exit

.P   E6(CR)      ;port 6, sector register
E6 XX  FF^       ;write to sector register
E6 FF  00^       ;verify write, clear sector register
E6 00  .         ;verify clear and exit

.P   E7(CR)      ;port 7, data register
E7 XX  FF^       ;write to data register
E7 FF  00^       ;verify write, clear data register
E7 00  .         ;verify clear and exit
```

If all of the above procedures give valid results, the FLP2 board is correctly interfaced to the STD-Z80 Bus.

2.8. CONNECTION OF FLP2 TO DISK DRIVE

The logic interconnection from FLP2 to the disk drive is made from J3 on the FLP2 board to the appropriate connection on the drive. The connection is made with a standard .1 inch center 50 pin ribbon cable. Refer to Figure 2-6.

Signal	Description	Pin Number
Drive Select 1,2,3,4	Output	26,28,30,32
Side Select	Output	14,48 (see note)
Step	Output	36
Write Data	Output	38
Write Gate	Output	40
Direction	Output	34
Head Load	Output	18
Read Data	Input	46
Index	Input	24 (5 in.) or 20 (8 in.)
Track 00	Input	42
Write Protect	Input	44
Drive Ready	Input	22

Note: Some 8" drives have an optional DATA SEPARATOR output on pin 48. If this is true on your drive, cut the etch on the FLP2 board going to pin 48 on J3.

Fig. 2-6: Cable Connection Pin Definitions for J3.

3. OEM GUIDE

This section serves as an OEM guide. The section begins with a discussion of the FLP2 port definitions. Also included is a discussion of both the MK3883 DMA Controller (DMAC) and the WD1797 Floppy Disk Controller (FDC). The section concludes with a design description of FLP2.

3.1. I/O PORTS

The MDX-FLP2 board occupies a block of eight contiguous I/O port addresses. This block of eight can be strapped anywhere in the main or IOEXP* address space. As shipped from the factory, the eight ports reside at E0H through E7H in the main port address space. Figure 3-1 shows the utilization of the eight ports.

	b7 b0	b7 b0
A2-A0	Read	Write
0 0 0	MK3883 DMA Controller IC	MK3883 DMA Controller IC
0 0 1	Undefined	Don't care
0 1 0	FB SZ - - - IR SS	Don't care
0 1 1	- - - - D4 D3 D2 D1	SD RS - - D4 D3 D2 D1
1 0 0	1797 Status Register	1797 Command Register
1 0 1	1797 Track Register	1797 Track Register
1 1 0	1797 Sector Register	1797 Sector Register
1 1 1	1797 Data Register	1797 Data Register

Where:

FB = 1 : FLP1 Board	FB = 0 : FLP2 board
SZ = 1 : 8 inch drive	SZ = 0 : 5 inch drive
IR = 1 : 1797 interrupt	IR = 0 : no 1797 IRQ
SS = 1 : 2-sided disk	SS = 0 : single sided
SD = 1 : single density	SD = 0 : double density
RS = 1 : 1797 active	RS = 0 : 1797 RESET
D4 = 1 : select drive four	D4 = 0 : no select
D3 = 1 : select drive three	D3 = 0 : no select
D2 = 1 : select drive two	D2 = 0 : no select
D1 = 1 : select drive one	D1 = 0 : no select

Fig. 3-1: Port Utilization on FLP2

3.1.1. Port 000 (xxxx x000)

Port 000 is assigned to the MK3883 DMA Controller chip. For a DMA data transfer operation, the DMA controller must be set up appropriately. For programmed data transfer in a polled environment, the DMA Controller need not be set up. For operation in an interrupt driven environment, the DMA Controller must be set up for interrupts; it is the only source of interrupts (the WD1797 INTRQ pin is connected to RDY on the DMA Controller). Setup and handling of the DMA Controller is covered in Section 3-2.

3.1.2. Port 001 (xxxx x001)

Port 001 is not used, but the MDX-FLP2 board will respond to a read command from the processor, although the data is undefined. Thus, this port may not be used for any other purpose.

3.1.3. Port 010 (xxxx x010)

Port 010 is a read-only port which presents four bits of information. The bits are defined as follows:

b6: 1 --> FLP1 board (single density)
    0 --> FLP2 board (single and double density)

b5: 1 --> 8 inch drives
    0 --> 5 1/4 inch drives

b1: 1 --> Interrupt request from 1797 floppy controller
    0 --> No interrupt request from 1797 floppy controller

b0: 1 --> Double-Sided Drives
    0 --> Single-Sided Drives

Note that b6 informs whether a MDX-FLP1 (single density) or a MDX-FLP2 (single and double density) board is in the system. This allows systems software to be written that handles either the FLP or the FLP2. Note that MDX-FLP1 only handles single density, while MDX-FLP2 handles both single and double density. Bit b5 indicates the drive size that FLP2 is strapped for (either 5 1/4 or 8 inch). Note that b6 and b5 are advisory flags to permit standard software to determine if FLP1 or FLP2 is in the system, as well as the drive size. This is to say, standard software may be written to handle both FLP1 and FLP2. In addition, b1 is useful when using FLP2 in a polled environment to check the status of the WD1797 IC. Finally, b0 is used to determine whether single or double sided disk drives are being used.

3.1.4. Port 011 (xxxx x011)

Writing into Port 011 affects drive selection, control, and WD1797 reset. Reading Port 011 returns the values for the drive selection and control bits. Disk drives are jumpered to interpret drive selection and control signals in various ways. Thus, the formal definition of these bits is as follows:

Port 011 Write:

b7: 1 --> Single Density
    0 --> Double Density

b6: 1 --> 1797 Reset Inactive
    0 --> 1797 Reset Asserted

b3: 1 --> Select Drive 4 (J3 pin 32)

b2: 1 --> Select Drive 3 (J3 pin 30)

b1: 1 --> Select Drive 2 (J3 pin 28)

b0: 1 --> Select Drive 1 (J3 pin 26)

Port 011 Read:

b3: 1 --> Drive 4 Selected
    0 --> Drive 4 Deselected

b2: 1 --> Drive 3 Selected
    0 --> Drive 3 Deselected

b1: 1 --> Drive 2 Selected
    0 --> Drive 2 Deselected

b0: 1 --> Drive 1 Selected
    0 --> Drive 1 Deselected

Note that forcing b6 low resets the 1797 chip. The advantage of a software reset is that the programmer has complete control. The programmer normally resets the 1797 once at power-up by setting b6 low, then setting b6 high.

For 5 1/4 inch drives with standard jumpering, a 1 on the drive select bit (b3, b2, b1 or b0) turns on the motor of all connected drives. When this bit is first set, a delay of one second is required before the drives can be used. Drive Select lines are used by setting the bit corresponding to the desired drive to a 1, the other bits to 0. Thus, up to four 8 inch drives or three 5 1/4 inch drives may be connected to FLP2. The Drive Select signals are cleared at power-up or system reset; thus a write to Port 011 to select the drive must be done before any

operation can be initiated. The 1797 Disk Controller knows nothing about selection and reselection of drives, which can cause problems if certain programming disciplines are not observed:

1. The drive selected should not be changed while an operation is in progress.

2. When a particular drive is first selected, either a Restore or a Read Address operation should be performed; this allows the head position to be "fixed."

3. When changing drive selection in a multi-drive system, the following steps are recommended:
   a. Output new drive selection to Port 011.
   b. Wait 35 milliseconds (70ms for 5 1/4 drive). This delay allows the Head Load output of the 1797 to become effective on the new drive. Note that the 35ms one-shot controlling Head Load timing is not effective in the case of drive reselection with the 1797 Head Load output true.
   c. Issue a Read Address command to Port 100. This is a data transfer command and DMA or programmed I/O provision must be made to read 6 bytes of data.
   d. On completion, if there are no errors, output the first byte of data (track number) to Port 101, the 1797 track register. If there were errors, issue a Restore command to Port 100.

3.1.5. Port 100 (xxxx x100)

Reading Port 100 clears INTRQ and/or acquires the 1797 Status Register. Refer to Section 3-3 for a discussion of the bit definitions of the 1797 registers.

Writing to Port 100 sends a command to the 1797. The commands are discussed in Section 3-3.

NOTE: Because of internal synchronization cycles, certain timing constrants must be followed, as shown in Figure 3-2.

Operation	Next Operation	Delay Required
Write to Command Register	Read Status Register	MFM = 14 usec FM = 28 usec
Write to Any Register	Read from a different Register	No delay

Note: Times double for 5 1/4 inch drives.

Fig. 3-2: WD1797 Timing Constrants

3.1.6. Port 101 (xxxx x101)

Port 101 is used to read and write to the eight-bit 1797 track register. The track register can be read at any time, although its contents during a Restore operation are not defined.

3.1.7. Port 110 (xxxx x110)

Port 110 is used to read and write the eight-bit 1797 sector register. The desired sector number is output to this port before issueing a Read or Write command. Note that the sector register is not updated by the 1797 except in "multiple sector" mode. It can be read at any time. The first sector on a track is 01.

3.1.8. Port 111 (xxxx x111)

Reading and writing Port 111 acceses the 1797 Data Register. When the DMA Controller is used to handle data transfers between the 1797 data register and RAM on the STD-Z80 Bus, the only use of Port 111 by the Z80 program is to write the destination track number into the Data Register prior to initiating a seek command.

3.2. MK3883 DMA CONTROLLER

As stated earlier, FLP2 may be used in either a polled or DMA driven environment. For DMA operation, FLP2 uses the powerful Z80-DMA Controller (MK3883), which operates at up to 4 Mhz. This section briefly describes programming the DMAC. In addition, example program segments show how to program the DMAC for use with FLP2.

3.2.1. Programming the Z80-DMA

The Z80-DMA has two programmable states: a enabled state and a disabled state. In the enabled state, the Z80-DMA can gain control of the system bus and transfer data between FLP2 and memory. In the disabled state, the Z80-DMA does not request the system bus.

At power-up or reset, the Z80-DMA is automatically placed in the disabled state. In addition, sending a command to the DMAC places it in the disabled state. The DMAC stays in the disabled state until receiving an "enable" command.

The DMAC is always programmed before transfer operations. To program, the CPU sends a sequence of control bytes using the Z80 OTIR instruction. When the DMAC receives the "enable" command, it may request the system bus when it is ready to transfer data.

Since the DMAC is such a powerful (hence complex) device, the examples below are helpful when writing DMA drivers for FLP2. For a complete discussion on the Z80-DMA, refer to the MOSTEK 1981 Z80 Microcomputer Data Book.

3.2.2. DMA Programming Examples

(To be supplied at a later date.)

3.3. WD1797 Floppy Disk Controller/Formatter

MDX-FLP2 uses the Western Digital WD1797 floppy disk controller chip. This chip generates the majority of signals required to transfer data, status, and control between the Z80 CPU and the disk drives.

The WD1797 contains five registers that are of interest to the programmer: Status, Command, Track, Sector and Data. Each of these registers is discussed below:

3.3.1. Status Register (Port xxxx x100, Read Only)

The status register holds the 1797 status information. The meaning of the status bits is a function of the Command register.

3.3.2. Command Register (Port xxxx x100, Write Only)

The command register holds the command being executed. This register should not be loaded when the device is busy.

3.3.3. Track Register (Port xxxx x101, Read and Write)

The track register holds the track number of the current Read/Write head position. It is incremented by one every time the head steps in; it is decremented by one when the head steps out (towards track 00). The contents of the register are compared with the recorded track number in the ID field during disk Read, Write and Verify operations. Do not load this register when the 1797 is busy. The track register is eight bits wide.

3.3.4. Sector Register (Port xxxx x110, Read and Write)

The sector registers holds the address of the desired sector position. The contents of the register are compared with the recorded sector number in the ID field during disk Read or Write operations. Do not load this register when the 1797 is busy. The sector register is eight bits wide.

3.3.5. Data Register (Port xxxx x111, Read and Write)

The data register is used as a holding register during disk read and write operations. In disk read operations, this register is read (usually by the DMA device) each time a byte of data is available from the disk. For a disk write operation, the register receives data (usually from the DMA) and sends it to the disk. When executing the Seek command, the data register holds the address of the desired Track position. The data register is eight bits wide.

3.3.6. Commands

The 1797 executes the eleven commands summarized in Figure 3-3. With the exception of the Force Interrupt command, a command is loaded into the internal Command Register only when bit 0 (BUSY) of the Status Register is inactive (low). During command execution, the BUSY bit is high. At command completion, or at an error condition, the INTRQ signal activates and the BUSY status bit goes low. The Status Register indicates if a completed command is in error or is fault free. As indicatated in Figure 3-3, the eleven commands executed by the 1797 are divided into four types. The following paragraphs describe the eleven commands under these four divisions.

Type	Command	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r1	r0
I	Seek	0	0	0	1	h	V	r1	r0
I	Step	0	0	1	u	h	V	r1	r0
I	Step-In	0	1	0	u	h	V	r1	r0
I	Step-Out	0	1	1	u	h	V	r1	r0
II	Read Sector	1	0	0	m	b	E	S	0
II	Write Sector	1	0	1	m	b	E	S	a0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0
IV	Force Interrupt	1	1	0	1	I3	I2	I1	I0

Fig. 3-3: WD1797 Floppy Controller Command Summary

3.3.7. Type I Commands

The Type I Commands include the Restore, Seek, Step, Step-In and Step-Out. Each of the Type I Commands contains a rate field (r1,r0) which determines the stepping motor rate. See Figure 3-3 for the Type I command summary.

Type I Commands also contain a head load flag (h), which determines when the head is loaded. If h=1, the head loads at the beginning of the command. Note that once the head loads, it remains enagaged until the 1797 receives a command that specifically unloads the head. If the 1797 is idle (BUSY=0) for 15 revolutions of the disk, the head automatically disengages.

The Type I Commands contain a verification flag (V). This flag determines if a verification operation is performed on the destination track. If V=1, a verification is performed; if V=0, no verification is performed. It is recommended to always keep verification enabled (V=1).

During verification, the head loads and after a 15ms delay, the head load input (HLT) is sampled. If HLT is active, the first encountered ID field is read off the disk. The track address of

the ID field is compared to the Track Register. If there is a match and a valid ID CRC, the verification is complete; an interrupt is generated and the BUSY status bit is reset. If there is not a match, but there is a valid CRC, an interrupt is generated and the Seek Error status bit (Status bit 4) sets while BUSY resets. If there is a match but not a valid CRC, the CRC error status bit sets (status bit 3), and the next encountered ID field is read. If an ID field with a valid CRC is not found after four revolutions, the 1797 terminates the operation and sends an interrupt.

The Step, Step-In and Step-Out commands contain an Update flag (u). When u=1, the track register is updated by one for each step. When u=0, the track register is not updated.

Note that the side select output (SSO) is not affected during Type I commands; an internal side compare does not take place when the verify flag (V) is on.

Restore (Seek Track 0)

The Restore command positions the head of the disk over track 0 (outer-most track). In addition, the track register loads with zeroes and an interrupt is generated. If the head is not over track 0, stepping pulses are sent at the rate specified in the r1,r0 field. If track 0 is not reached after 255 stepping pulses, the 1797 terminates the operation, interrupts, and sets the Seek Error status bit.

A verification operation occurs during Restore if the verify flag (V) is set. The h bit allows the head to be loaded at the start of the command. Note that the Restore command is executed when the 1797 is Reset (forcing bit 6 of port 010 low and then high).

Seek

The Seek command assumes that the Track Register contains the track number of the current position of the Read/Write head; the Data register contains the desired track number. The 1797 issues stepping pulses in the appropriate direction until the contents of the Track register are equal to the contents of the Data Register. A verify operation occurs if the V flag is set. The h bit allows the head to load at the start of the command (h=1). An interrupt occurs at the completion of the command.

Step

The Step command issues stepping pulses to the disk drive. The stepping direction is the same as in the previous step command. After a delay determined by the r1,r0 field, a verify operation occurs if the V flag is set. If the u flag is set, the Tratk Register is updated. If the h bit is set, the head loads at the start of the command. An interrupt occurs at command completion.

Step-In

The Step-In command issues one stepping pulse in the direction towards track 76 (the inner-most track). If the u flag is set, the Track Register is incremented by one. After a delay determined by the r1,r0 field, a verify operation occurs if the V flag is set. Setting the h bit loads the head at the start of the command. An interrupt occurs at command completion.

Step-Out

The Step-Out command issues one stepping pulse in the direction towards track 0 (the outer-most track). If the u flag is set, the track register is decremented by one. After a delay determined by the r1r0 field, a verify operation occurs if the V flag is set. Setting the h bit loads the head at the start of the command. An interrupt occurs at command completion.

3.3.8. Type II Commands

The Type II commands are the Read Sector and Write Sector commands. Prior to loading the Type II command into the Command Register, the computer must load the sector register with the desired sector number. Upon receipt of the Type II command, the Busy status bit sets. If the E flag is one (this is the normal case) head load (HLD) is activated and head loaded (HLT) is sampled after a 15ms delay. If the E flag is 0, the head loads and HLT is sampled with no 15ms delay.

When an ID field is located on the disk, the 1797 compares the track number on the ID field with the track register. If there is not a match, the next encountered ID field is read and a comparison is again made. If there is a match, the sector number of the ID field is compared with the sector register. If there is not a sector match, the next encountered ID field is read off the disk and comparisons again made. If the ID field CRC is correct, the data field is then located and is either written into, or read from, depending on the command. The 1797 must find an ID field with a track number, sector number, side number, and CRC within four revolutions of the disk; otherwise, the Record Not Found status bit is set (status bit 3) and the command terminates with an interrupt.

Each of the Type II commands contains a flag which determines if mutiple records (sectors) are to be read or written. If m=0, a single sector is read or written and an interruption occurs at command completion. If m=1, multiple sectors are read or written with the sector register internally updated so that an address verification can occurs on the next sector. The 1797 continues to read or write multiple sectors and updating the sector register until the sector register exceeds the number of sectors on the track or until the Force Interrupt command is loaded into the command register, which terminates the command and generates an interrupt.

If the sector register exceeds the number of sectors on the track, the Record-Not-Found status bit is set.

The Type II commands also include a b flag. The b flag, in conjunction with the sector length byte of the ID field, allow different byte length to be implemented in each sector. For IBM compatability, the b flag is set to 1.

The s flag allows direct control over the side select output. Side 0 or Side 1 is selected, depending on the value of this flag.

Read Sector

Upon receipt of the Read Sector command, the head loads and the Busy status bit sets. When encountering an ID field that has the correct track number, sector number, side number and CRC, the data field is presented to the computer. The Data Address Mark of the data field must be found within 30 bytes in single density and 43 bytes in double density of the last ID field CRC byte; if not, the Record Not Found status bit sets and the operation terminates.

When the first byte of the data field is ready, a data request (DRQ) is generated. When the next byte is ready, another DRQ is generated. If the computer does not read the previous contents of the data register before the next byte is ready, the byte is lost and the Lost Data bit sets. This sequence continues until the complete data field is input to the computer. If there is a CRC error at the end of the data field, the CRC error status bit sets, and the command terminates (even if it is a mutiple record command).

At the end of the Read operation, the type of Data Address Mark encountered in the data field is recorded in the status register (bit 5) as shown below:

. status bit 5 = 1 --> Deleted Data Mark

. status bit 5 = 0 --> Data Mark

Write Sector

The Write Sector command loads the head (HLD active) and sets the busy bit. When encountering an ID field that has the correct track number, sector number, side number and CRC, a data reguest (DRQ) is generated. The 1797 counts off 11 bytes in single density and 22 bytes in double density from the CRC field and the Write Gate (WG) output is activated is the DRQ is serviced (i.e., the DR is loaded by the computer). If DRQ has not been serviced, the command is terminated and the Lost Data status bit sets. If the DRQ is serviced, the WG is activated and six bytes of zeros (single density) or 12 bytes of zeros (double density) are then written on the disk. At this time the Data Address Mark is written on the disk as determined by the a0 field of the command:

a0 = 1 --> Deleted Data Mark

a0 = 0 --> Data Mark

The 1797 then writes the data field and generates DRQ's to the computer. If the DRQ is not serviced in time for continuous writing, the Lost Data Status bit sets and a byte of zeros is written on the disk. The command is not terminated. After the last data byte is written , the two-byte CRC is computed internally and written on the disk followed by one byte of logic ones in FM or in MFM. The WG output is then deactivated.

3.3.9. Type III Commands

Read Address

The Read Address command loads the head and sets the Busy Status bit. The next encountered ID field is then read in from the disk, and the six data bytes of the ID field are assembled and transferred to the data register; a DRQ is generated for each byte. The six bytes of the ID field are shown below:

Byte 1. Track Address
Byte 2. Side Number
Byte 3. Sector Address
Byte 4. Sector Length
Byte 5. CRC 1
Byte 6. CRC 2

Although the CRC bytes are tranferred to the computer, the 1797 checks for validity. The CRC error status bit sets if there is a CRC error. The track address of the ID field is written into the sector register. At the end of the operation an interrupt occurs and the Busy status is reset.

Read Track

The Read Track command loads the head and sets the Busy status bit. Reading starts with the leading edge of the first encountered index pulse and continues until the next index pulse. As each byte is assembled, it is transferred to the data register and the data request is generated for each byte. No CRC checking is performed. Gaps are included in the input data stream. The accumulation of bytes is synchronized to each Address Mark encountered. Upon completion of the command, the interrupt is activated. Read Gate is not activated during the Read Track command. An internal side compare is not performed during a read track.

Write Track

The Write Track command loads the head and sets the Busy status bit. Writing starts with the leading edge of the first encountered index pulse and continues until the next index pulse, at which time the interrupt is activated. The data request activates immediately upon receiving the command, but writing does not start until after the first byte is loaded into the data register. If the data register is not loaded by the time the index pulse is encountered, the operation terminates, making the device Not Busy, the Lost Data status bit set and the interrupt set. If a byte is not present in the data register when needed, a byte of zeros is substitued. Address Marks and CRC characters are written on the disk by detecting certain data byte pattern in the outgoing data stream. This is shown below. The CRC generator initializes when any data byte from F8 to FE is about to be transfered from the data register to the data shift register in FM or by receipt of F8 in MFM.

Data Pattern in Data Register	1797 Interpretation in FM (Single Density)	1797 Interpretation in MFM (DB Density)
00 thru F4	Write 00 thru F4	Write 00 thru F4
F5	Not Allowed	Write A1,Preset CRC
F6	Not Allowed	Write C2
F7	Generate 2 CRC bytes	Generate 2 CRC byte
F8 thru FB	Write F8 thru FB	Write F8 thru FB
FC	Write FC	Write FC

3.3.10. Type IV Command

The force interrupt command can be loaded into the command register at any time. If there is a current command under execution (BUSY status bit set), the command is terminated and an interrupt is generated when the condition specified in the I0 through I3 field is detected. The interrupt conditions are shown below:

I0 = Not Ready To Ready Transition
I1 = Ready to Not Ready Transition
I2 = Every Index Pulse
I3 = Immediate Interrupt (reguires reset, see note)

Note: If I0-I3 = 0, there is no interrupt generated but the current command is terminated and busy is reset. This is the only command that will enable the immediate interrupt to clear on a subsequent Load Command Register or Read Status Register.

Status

If the Force Interrupt command is received when there is a current command under execution, the BUSY status bit is reset, and the rest of the status bits are unchanged. If the Force Interrupt command is received when there is not a current command under execution, the BUSY status bit is reset and the rest of the status bits are updated or cleared. In this case, Status reflects the Type I commands.

3.4. Formatting A Disk

Formatting a disk is accomplished by positioning the R/W head over the desired track and issuing the Write Track command. Upon receipt of the Write Track command, the 1797 raises the Data Request signal. At this point, the user loads the data register with desired data to be written to disk. For every byte of information to be written, a data request is generated. This sequence continues from one index mark to the next index mark. Normally, whatever data pattern appears in the data register is written on the disk. However, if the 1797 detects a data pattern of F5 thru FE in the data register, this is interpreted as data address marks with missing clocks or CRC generation. For example, in FM an FE pattern is interpreted as an ID address mark (Data FE, Clock C7) and the CRC is initialized. An F7 pattern generates two CRC characters in FM or MFM. As a consequence, the patterns F5 thru FE must not appear in the gaps, data fields, or ID fields. Also, CRC's must be generated by an F7 pattern.

Disks are formatted in IBM 3740 or System 34 formatted with sector lengths of 128, 256, 512 or 1024 bytes.

3.4.1. IBM 3740 Format - 128 Bytes/Sector

Shown below is the IBM single-density format with 128 bytes/sector. In order to format a diskette, the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

	Number of Bytes	Hex Value of Byte Written
	40	FF or 00 (Mostek uses 00)
	6	00
	1	FC (Index Mark)
	26	FF or 00 (Mostek uses 00)
*	|---- 6	00
	| 1	FE (ID Address Mark)
	| 1	Track Number
	| 1	Side Number (00 or 01)
	| 1	Sector Number (1 thru 1A)
	| 1	00
	| 1	F7 (Two CRC's written)
	| 11	FF or 00 (Mostek uses 00)
	| 6	00
	| 1	FB (Data Address Mark)
	| 128	Data (IBM uses E5)
	| 1	F7 (Two CRC's written)
	|--- 27	FF or 00 (Mostek uses 00)
	247 Plus	Continue writing until 1797 Interrupts Out (Approx. 247 bytes)

* Write Bracked field 26 times

3.4.2. IBM System 34 Format - 256 Bytes/Sector

Shown below is the IBM dual-density format with 256 bytes/sector. In order to format a diskette the user must issue the Write Track command and load the data register with the following values. For every byte to be written, there is one data request.

	Number of Bytes	Hex Value of Byte Written
	80	4E
	12	00
	3	F6
	1	FC (Index Mark)
	50	4E
* |---	12	00
|	3	F5
|	1	FE (ID Address Mark)
|	1	Track Number (0 thru 4C)
|	1	Side Number (0 or 1)
|	1	Sector Number (1 thru 1A)
|	1	01
|	1	F7 (Two CRC's written)
|	22	4E
|	12	00
|	3	F5
|	1	FB (Data Address Mark)
|	256	Data
|	1	F7 (Two CRCs written)
|---	54	4E
	598	4E (Continue writing until 1797 interrupts out; approx. 589 bytes)

* Write bracketed field 26 times

Type I Command Summary

Type	Command	7	6	5	4	3	2	1	0
I	Restore	0	0	0	0	h	V	r1	r0
I	Seek	0	0	0	1	h	V	r1	r0
I	Step	0	0	1	u	h	V	r1	r0
I	Step-In	0	1	0	u	h	V	r1	r0
I	Step-Out	0	1	1	u	h	V	r1	r0

Where:

h = Head Load Flag (Bit 3)

h = 1 ; Load head at beginning
h = 0 ; Unload head at beginning

V = Verify Flag (Bit 2)

V = 1 ; Verify on destination track
V = 0 ; No verify

u = Update flag (Bit 4)

u = 1 ; Update track register
u = 0 ; No update

r1,r0 = Stepping Rates

Drive Size	8	8	5 1/4	5 1/4
DDEN*	0	1	0	1
r1,r0				
0 0	3ms	3ms	6ms	6ms
0 1	6ms	6ms	12ms	12ms
1 0	10ms	10ms	20ms	20ms
1 1	15ms	15ms	30ms	30ms

Fig. 3-4: Type I Command Summary

Type II and III Command Summary

Type	Command	7	6	5	4	3	2	1	0
II	Read Sector	1	0	0	m	b	E	S	0
II	Write Sector	1	0	1	m	b	E	S	a0
III	Read Address	1	1	0	0	0	E	0	0
III	Read Track	1	1	1	0	0	E	0	0
III	Write Track	1	1	1	1	0	E	0	0

Where:

m = Multiple Record Flag (Bit 4)

m = 1 ; Multiple Records
m = 0 ; Single Record

a0 = Data Address Mark (Bit 0)

a0 = 1 ; Deleted Data Mark (F8)
a0 = 0 ; Data Mark (FB)

E = 15ms Delay (2Mhz)

E = 1 ; 15ms Delay
E = 0 ; No 15 ms Delay

S = Side Select Flag

S = 1 ; Select Side 1
S = 0 ; Select Side 0

b = Sector Length Flag

	Sector Length Field			
	00	01	10	11
b = 0	256	512	1024	128
b = 1	128	256	512	1024

Fig. 3-5: Type II and III Commands

Type IV Command Summary

Type	Command	7	6	5	4	3	2	1	0
IV	Force Interrupt	1	1	0	1	I3	I2	I1	I0

Where:

```
In = Interrupt Condition Flags
------------------------------
I3 = 1     ; Immeditate Interrupt
I2 = 1     ; Index Pulse
I1 = 1     ; Ready to Not-Ready Transition
I0 = 1     ; Not-Ready to Ready Transition
I3-I0 = 0  ; Terminate with no Interrupt
```

Fig. 3-6: Type IV Command Summary

3.5. MDX-FLP2 DESIGN DESCRIPTION

This section describes the hardware design of MDX-FLP2.

It is important to understand the conventions used throughout this section. All signals that are active low are represented by a "(L)" following the signal name, i.e., RD(L), WR(L), and IOEXP(L). Signals that are active high are followed by a "(H)." Signals followed by a "*," are active high and low, but are inverted, i.e. CLK*. Signals not followed by any of the preceding are noninverted, active high and low, i.e. A0-A15 and D0-D7.

3.5.1. Functional Block Description

A block diagram of FLP2 is shown in Figure 3-7. The basic blocks consist of:

- Bus Buffers
- Port Selection Logic
- Bus Direction/Control Logic
- Status/Command Ports
- WD1797 Floppy Controller IC
- Head Load Timing
- Write Precomp/Data Separator Logic
- Read Pulse Shaper
- DMA Control
- MK3883 DMA Controller
- DMA Daisy Chain Logic

The following discussion describes the operation of each block.

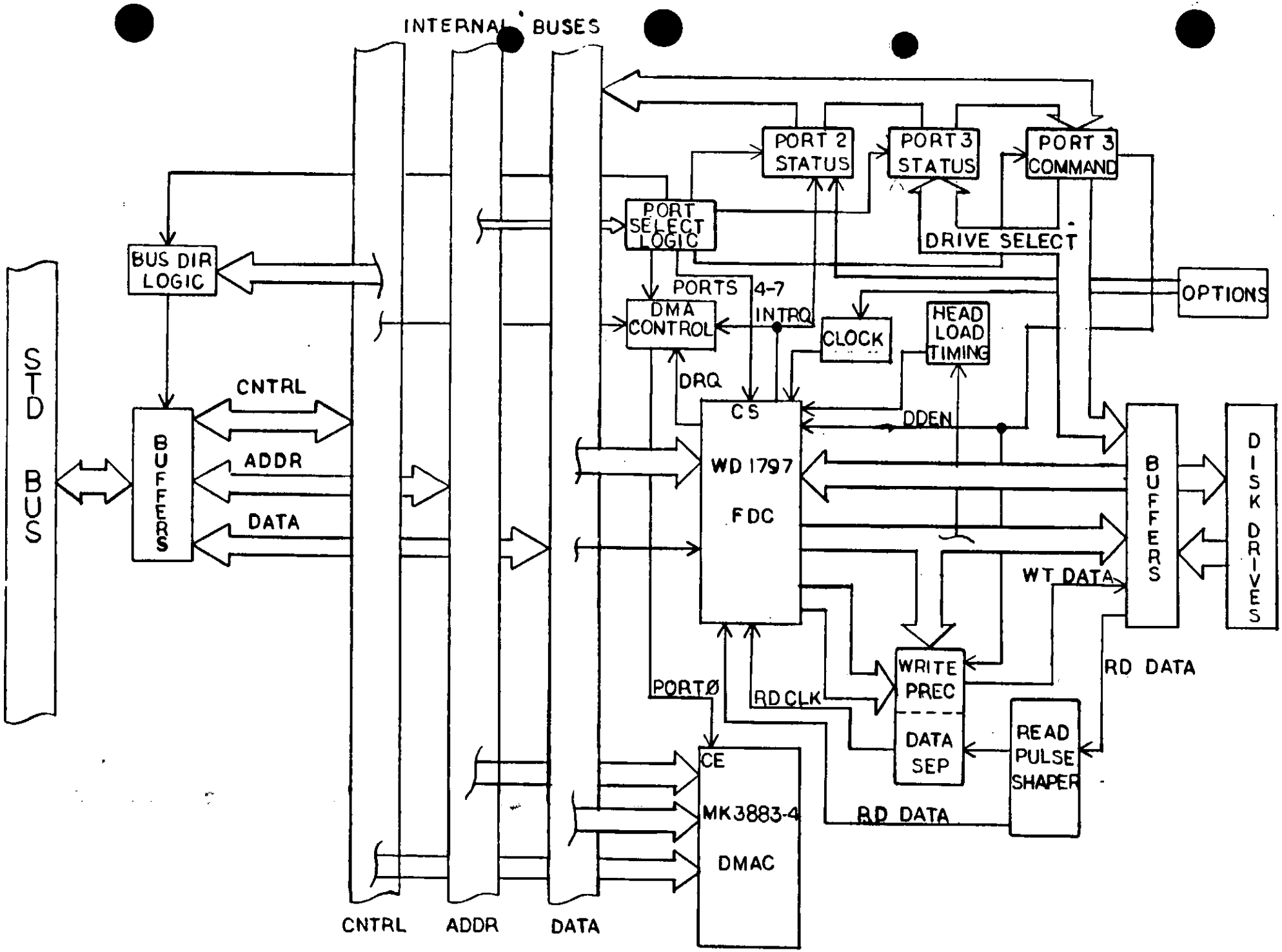


FIG. 3-7: MDX-FLP2 BLOCK DIAGRAM

3.5.2. Bus Buffers

The bus buffers interface FLP2 to the STD-Z80 bus. Address lines A15-A8 are buffered by U27, a 74LS244, while A7-A0 are buffered by U26, a 74LS245. Note that U27 is enabled only when the MK3883 DMA Controller (DMAC) is bus master. U26 normally functions as a receiver on FLP2; the exception is when the DMAC is bus master, which causes U26 to function as a driver onto the STD-Z80 bus.

The eight data lines (D7-D0) are buffered by U25, a 74LS245. The 74LS245 functions as a driver or receiver, depending on the levels of RD(L) and WR(L). U25 is always enabled.

Bus control lines IORD(L), IOWR(L), IORQ(L) and MREQ(L) are buffered by U29, a 74LS243. U29 normally functions as a receiver for FLP2; when the DMAC controls the bus, U29 is a driver onto the STD-Z80 bus.

Bus control lines M1(L), BUSAK(L), PCI, WAIT(L), INTAK(L) and SYSRESET(L) are buffered by U30, a 74LS244. Note that U24 is always enabled -- the DMAC does not use these signals when it is bus master. In addition, bus signals BUSRQ(L), INTRQ(L) and PCO(H) are driven onto the bus by various gates.

3.5.3. Port Select Logic

The port select logic enables the required data, status or command port when a valid port address appears on the bus. The main components are U14, a DM8131 (a 6-bit comparator), and U13, a 74LS138 (a 3-to-8 decoder). The 6-bit comparator compares address lins A7-A3 to the port select address strapped at J7. In addition, one bit of the comparator may be strapped to watch for either a high or low on IOEXP(L). Normally, IOEXP is not used, in which case J6, pins 2 and 3, are strapped.

Assuming a valid address, the 6-bit comparator output (PORT SEL low) enables the LS138. Also, PORT SEL(L) goes to U4, a 74LS32 and U17, a 74LS27. With the LS138 enabled, address lines A0 and A1 are used to produce three signals: PORT0 SEL(L); PORT2 SEL(L); and PORT3 SEL(L). PORT0 SEL(L) enables the DMAC unless the DMAC is bus master; in this case PORT0 SEL(L) is disabled by a 74LS125, U21. The 74LS125 multiplexes WAIT(L) and PORT SEL(L).

PORT2 SEL(L) gates with IORD(L) -- by way of U4, a LS32 -- to produce RD PORT2(L). Similarly, PORT3 SEL(L) gates with IORD(L) to produce RD PORT3(L); PORT3 SEL(L) gates with IOWR(L) to produce WR PORT3(L).

In addition, PORT SEL(L) and A2 produce floppy disk controller select (FDC SEL low). A0 and A1 are sent to the floppy controller for internal decoding.

3.5.4. Bus Direction Logic

The bus direction logic control the direction of the data, address and control buffers. This is necessary since, although the CPU is normally bus master, the DMAC also may become bus master. Thus, although the address lines normally driven onto FLP2, the address and control lines are driven out of FLP2 when the DMAC aquires the bus.

The ICs affected by the bus direction control logic are the data buffers (U25, a 74LS245), the addrress buffers (U26, a 74LS245 and U27, a 74LS244), and the control buffers (U29, a 74LS243). The direction of the buffers is controlled by the signal ADDROUT(H) and its complement, ADDROUT(L).

3.5.5. Head Load Timing

The head load timing circuit is concerned with delaying the Head Loaded (HLT) signal to the WD1797. The circuit uses 1/2 of U15, a 74LS221, connected as a monostable. The Head Load (HLD) signal from the WD1797 triggers the monostable. After a delay of approximately 43ms, the output of the 74LS221 goes low, causing the HLT input to sense that the head is loaded. Note that the HLD signal also goes directly to the floppy disk drive.

3.5.6. Read Pulse Shaper

The read pulse shaper logic uses the other half of the 74LS221, U15. Since the duration of the read pulse varies from drive to drive, the74LS221 shapes the pulse for the WD1797. Regardless of the actual shape of the pulse coming from the drive, the 74LS221 produces a 117 nsec pulse. Thus, the data separation logic always "sees" the same duration read pulse, allowing the data separation logic to be "fine tuned." Note that the pulse output goes directly to the WD1797 and the WD1696.

3.5.7. Write Precompensation/Data Separator Logic

All of the write precompensation logic and most of the data separation logic are contained in the Western Digital chip sets; WD1797, WD1691; and WD2143. The write precompensation is accomplished completely internal to these ICs. Note that the auto precomp is a strapable option, by way of J4.

Data separation is accomplished internal to the WD1797. However, for correct operation, the RCLK input must be in phase with the incoming raw read data. RCLK stays in phase under control of the WD1691 floppy support IC.

The WD1691 observes the incoming raw data and issues PU (pump up) and PD (pump down), which are tied directly to the voltage controlled oscilator (U9, a 74LS624). The output of the

VCO is 4 Mhz for 8 inch drives, but may be divided by U19, 1/2 a 74LS74, to obtain 2 Mhz for 5 1/4 inch drives. The WD2143 is a multiphase clock IC required for correct operation of the WD1697.

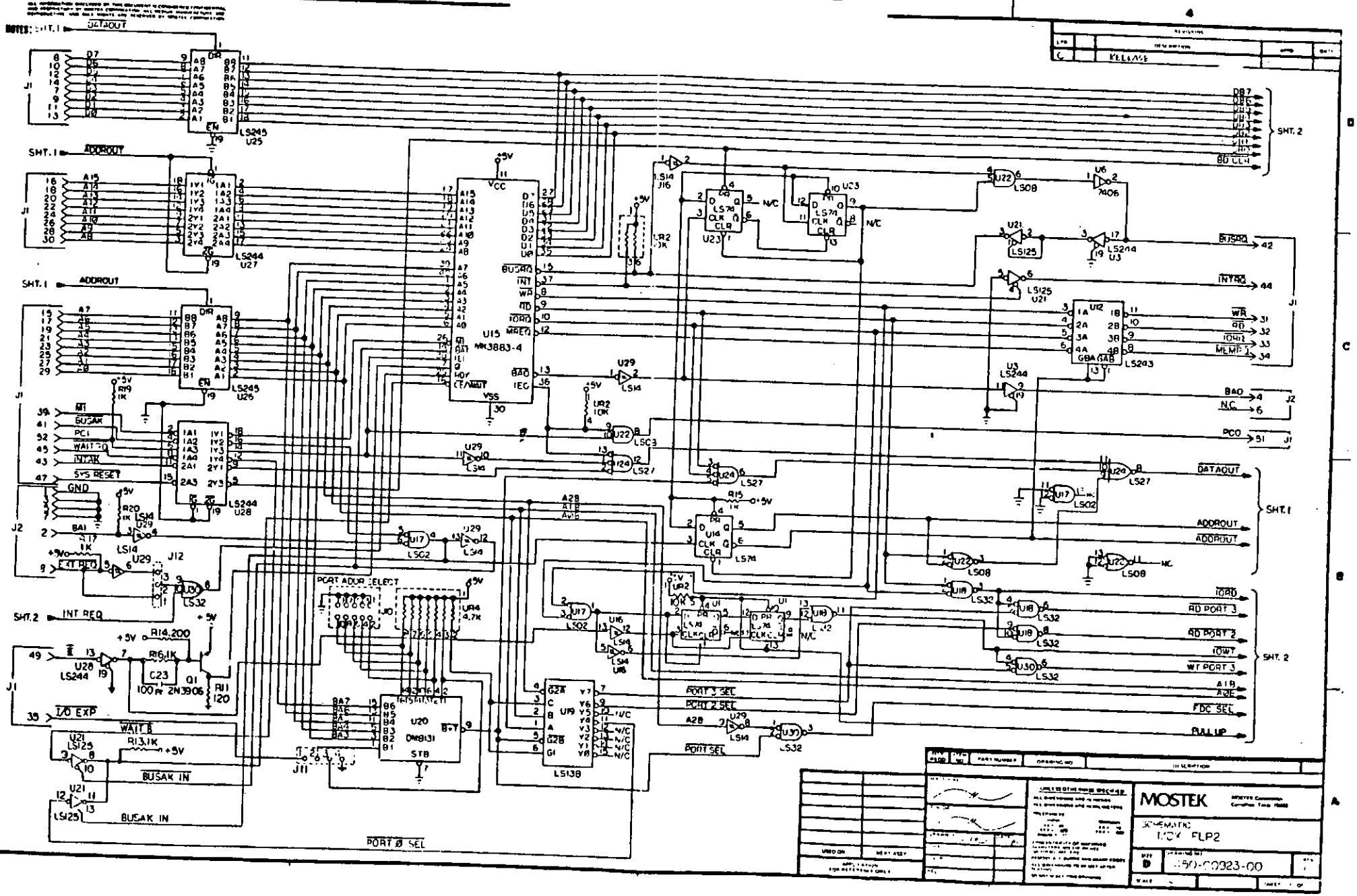
3.5.8. Daisy Chain Priority DMA Logic

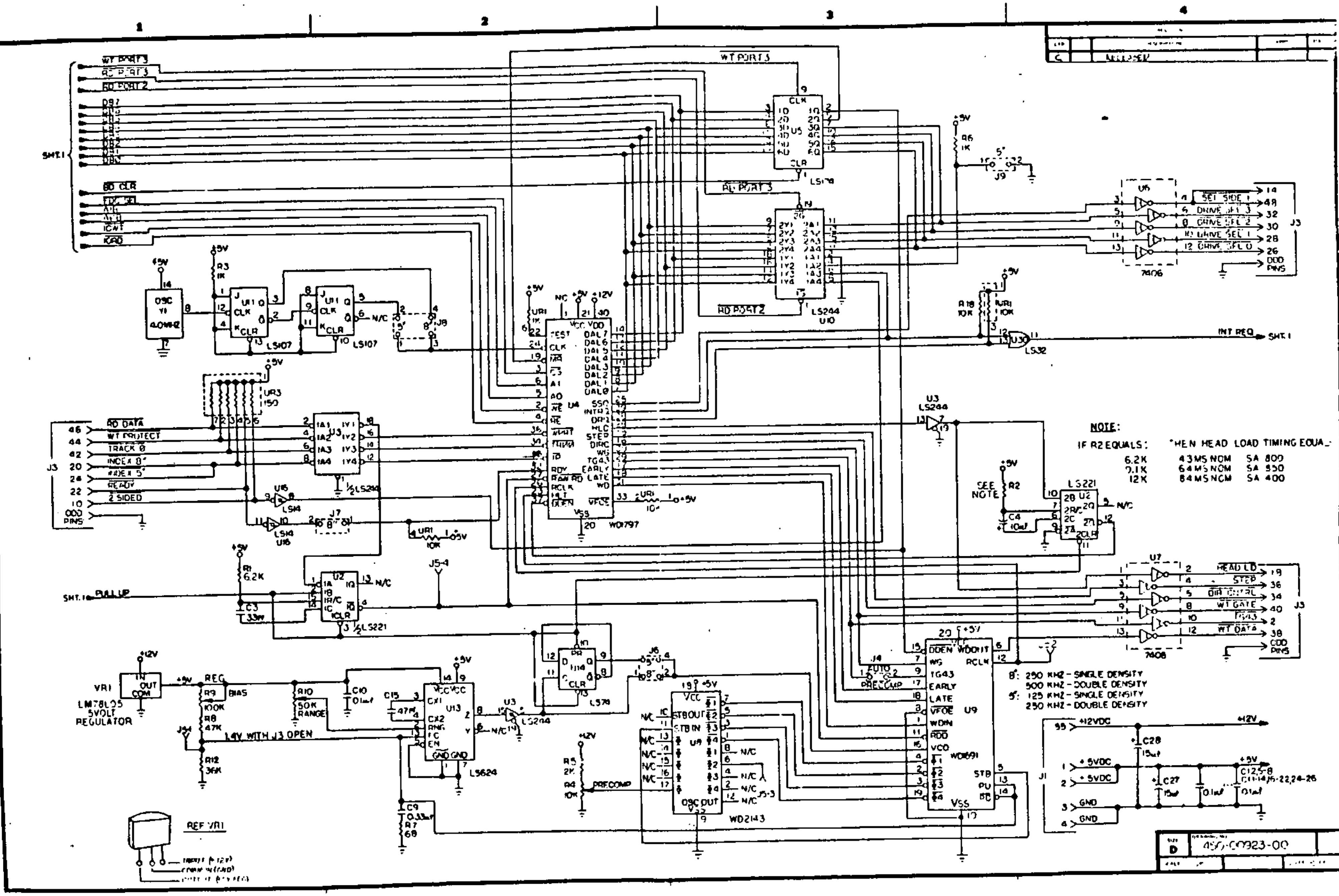
FLP2 has the ability of operating with multiple bus masters. By including a DMA daisy chain, multiple DMA devices may be prioritized on the bus.

Two non STD-Z80 bus signals are used to implement the DMA bus daisy chain. These are accessed from the eight pin connector on top ot the FLP2 board (J2). The two signals are Bus Available In (BAI(H)) and Bus Available Out (BAO(H)). In addition, the External DMA Request input is on J2. Note that EXTREQ may be strapped for either active HIGH or active LOW operation, by way of J12. EXTREQ is connected to the READY input of the DMAC.

Note that BAI(H), BAO(H) and EXTREQ are not on the STD-Z80 bus. Instead, they are jumpered (using an eight pin connector) from each board in the daisy chain. Also, note that BAI and BAO are used with BUSRQ(L) and BUSAK(L), which are included on the STD-Z80 bus.

A. Schematic and Parts List




WT PORT 3
RD PORT 3
RD PORT 2
SHT 1
BD CLR
INT REQ
U5 LS174
U10 LS244
U6 7406
SEL SIDE 1
DRIVE SEL 3
DRIVE SEL 2
DRIVE SEL 1
DRIVE SEL 0
ODD PINS
J3
J9
OSC Y1 4.0MHZ
U11 LS107
J8
U4 WD1797
U3 LS32
U3 LS244
NOTE:
IF R2 EQUALS: THEN HEAD LOAD TIMING EQUA..
6.2K 43MS NOM SA 800
9.1K 64MS NOM SA 850
12K 84MS NOM SA 400
SEE NOTE
LS221
RD DATA
WT PROTECT
TRACK 0
INDEX 8"
INDEX 5"
READY
2 SIDED
UR3 150
1/2 LS244
U16 LS14
J7
J5-4
SHT.1 PULLUP
1/2 LS221
U7 7406
HEAD LD
STEP
DIR CNTRL
WT GATE
TG43
WT DATA
VR1
LM78L05 5VOLT REGULATOR
REG
BIAS
50K RANGE
1.4V WITH J3 OPEN
U13 LS624
LS74
PRECOMP
WD2143
U9 WD1691
8": 250 KHZ - SINGLE DENSITY
500 KHZ - DOUBLE DENSITY
5": 125 KHZ - SINGLE DENSITY
250 KHZ - DOUBLE DENSITY
+12VDC
+5VDC
GND
J1
REF VR1
D
450-00923-00

0000000		PARTS LIST MDX-FLP2	
0000001		SCHEMATIC DWG.	450-00923-00 C
0000002		ASSY,PWA 8" FLP INTRFACE DWG	450-00922-10 C
4610303	1	PWB MDX FLP2 PCB REV A	DWG 450-00921-10 C
4150174	21	CAP 0.1 UF 50 V CER Z5U DIP	C1,2,5-8,10-14,16-22 C24-26
4150086	1	CAP 33. PF 500 V MICA 5%	C3
4150166	1	CAP 10. UF 20 V TANT 10% AX	C4
4150213	1	CAP .33UF 50 V CER 20% .2	C9
4150223	1	CAP 47. PF 200 V CER 10%NPO	C15
4150090	1	CAP 100. PF 300 V MICA 5%	C23
4150140	2	CAP 15. UF 20 V ALEL 20%	C27,28
4210432	1	HEADER 8P 2 X 4 RA TIN	J2
4210229	1	CONN HDR 50 POS ST RA LP	J3
4210087	3	HEADER 2P 2 X 1 ST TIN	J4,7,9
4210402	2	HEADER 4P 4 X 1 ST TIN	J5,11
4210238	2	HEADER 4P 2 X 4 ST TIN	J6,8
4210144	1	HEADER 10P 2 X 5 ST TIN	J10
4210478	1	HEADER 3P 3 X 1 ST TIN	J12
4480011	1	TRANS 2N3906 PNP SWITN	Q1
4470092	2	RES 6.2 KOHM 1/4W 5% CAR	R1,R2(SEE*)
4470073	8	RES 1. KOHM 1/4W 5% CAR	R3,6,13,15-17,19-20
4475031	1	RES 10. KOHM POT 25T	R4
4470080	1	RES 2. KOHM 1/4W 5% CAR	R5
4470045	1	RES 68. OHM 1/4W 5% CAR	R7
4470113	1	RES 47. KOHM 1/4W 5% CAR	R8
4475030	1	RES 100. KOHM POT	R9
4475029	1	RES 50. KOHM POT	R10
4470051	1	RES 120. OHM 1/4W 5% CAR	R11
4470110	1	RES 36. KOHM 1/4W 5% CAR	R12
4470056	1	RES 200. OHM 1/4W 5% CAR	R14
4470097	1	RES 10. KOHM 1/4W 5%	R18
4313413	3	IC TTL 74LS74 DUAL D F/F	U1,14,23
4313638	1	IC TTL 74LS221 DUAL 1 SHOT	U2
4313507	4	IC TTL 74LS244 OCT BUF TS	U3,10,27,28
4312002	1	IC MOS WD1797B FLP CNTL DD/DS	U4
4313305	1	IC TTL 74LS174 HEX D F/F	U5
4313008	2	IC TTL 7406 HEX INV OC	U6,7
4312004	1	IC MOS WD2143-03 4PHASE CLK	U8
4312003	1	IC MOS WD1691 FLP SUP LOGC	U9
4313716	1	IC TTL 74LS107 DUAL JK F/F	U11
4313562	1	IC TTL 74LS243 4 BUS TCVR	U12
4312041	1	IC TTL 74LS624 VOLT CNTL OSC	U13
4312026	1	IC MOS MK3883-4 Z80A-DMA	U15
4313291	2	IC TTL 74LS14 HEX INV ST	U16,29
4313300	1	IC TTL 74LS02 4 2INP NOR	U17
4313411	2	IC TTL 74LS32 4 2INP OR	U18,30
4313296	1	IC TTL 74LS138 3 TO 8 DMUX	U19
4313749	1	IC TTL DM8131 6 BIT COMP	U20

SIZE	FSCM	DRAWING NO.
A	50088	
SCALE		SHEET OF

4313641	1	IC TTL 74LS125 4 BUFR TS	U21
4313289	1	IC TTL 74LS08 4 2INP AND	U22
4313501	1	IC TTL 74LS27 3 3INP NOR	U24
4313508	2	IC TTL 74LS245 8 BUS TCVRTS	U25,U26
4470293	2	RES 10. KOHM 6P/5R SIP 5%	UR1,2
4470275	1	RES 150. OHM 8P/7R SIP 5%	UR3
4470330	1	RES 4.7 KOHM 8P/7R SIP 5%	UR4
4312027	1	IC LIN LM78L05 5V REG CAN	VR1
4620019	2	SOCKET IC 40 PIN DIP LP	X4,15
4620101	1	SOCKET IC 18 PIN DIP LP	X8
4620070	1	SOCKET IC 20 PIN DIP LP	X9
4620145	1	SOCKET RES 2 PIN SIP 6P 2P LOD	XR2 INSERT B 4 R2
4313184	1	OSC MOD 4.0000 MHZ	Y1
4280155	1	EJECTOR,CARD	Z0:
4210244	7	CONN MINI JUMPER	Z1:INSTALLED AT TEST

******* XR2 IS INSTALLED BEFORE R2 IS INSTALLED. *******

B. STD-Z80 Bus Signals Used By MDX-FLP2

The following is a list of STD-Z80 Bus signals used by the MDX-FLP2 board. Pin numbers without a description are not used by MDX-FLP2. Signals followed by an "(L)" are active LOW, while signals followed by an "(H)" are active HIGH. Signals followed by a "*" are active high and low, but are inverted, i.e., CLK*. All other signals are noninverted, active high and low. The signals are accessed via J1, a 56 pin PC edge connector.

Pin	Mnemonic	Description	Pin	Mnemonic	Description
1	+5	+5 Vdc system power	2	+5	+5 Vdc system power
3	GND	System ground	4	GND	System ground
5			6		
7	D3	Data bit 3	8	D7	Data bit 7
9	D2	Data bit 2	10	D6	Data bit 6
11	D1	Data bit 1	12	D5	Data bit 5
13	D0	Data bit 0	14	D4	Data bit 4
15	A7	Address bit 7	16	A15	Address bit 15
17	A6	Address bit 6	18	A14	Address bit 14
19	A5	Address bit 5	20	A13	Address bit 13
21	A4	Address bit 4	22	A12	Address bit 12
23	A3	Address bit 3	24	A11	Address bit 11
25	A2	Address bit 2	26	A10	Address bit 10
27	A1	Address bit 1	28	A9	Address bit 9
29	A0	Address bit 0	30	A8	Address bit 8
31	WR(L)	Write	32	RD(L)	Read
33	IORQ(L)	IO Request	34	MEMRQ(L)	Memory Request
35	IOEXP(L)	IO Expand	36		
37			38		
39	M1(L)	Machine Cycle	40		
41	BUSAK(L)	Bus Acknowledge	42	BUSRQ(L)	Bus Request
43	INTAK(L)	Interrupt Acknowledge	44	INTRQ(L)	Interrupt Request
45	WAITRQ(L)	Wait Request	46		
47	SYSRST(L)	System Reset	48		
49	CLOCK(L)	System Clock	50		
51	PCO(H)	Priority Chain Out	52	PCI(H)	Priority Chain In
53			54		
55	+12	+12 Vdc system power	56		

C. Differences Between FLP1 and FLP2

For those customers presently using FLP1 and are upgrading to FLP2, the main differences between the two are as follows:

1. FLP1 is for single density only, while FLP2 handles both single and double density.

2. FLP1 may only be used in 2.5 Mhz systems, while FLP2 can be used in 2.5 or 4.0 Mhz systems.

3. The side select (SS) bit is at port 3, bit 4 on the FLP1; SS is bit 1 on the READ SECTOR and WRITE SECTOR commands sent to the FLP2 board. (See page 20, Figure 3-3, WD1797 Floppy Controller Command Summary.)

4. The FLP1 powers-up in the initialized state, while FLP2 powers-up in the RESET state. To remove FLP2 from the reset state, set bit 6 of port 3 to a 1. (See page 15, Section 3.1.4 for more information.)

D. References

1. Mostek 1981 Z80 Microcomputer Data Book
   Publication Number MK79602

2. Western Digital FD1797 Data Sheet

3. Shugart SA851 Floppy Disk Drive Manual