DEC-8I-H8NA-D

KT8/I
TIME-SHARING OPTION
FUNCTIONAL DESCRIPTION

DIGITAL EQUIPMENT CORPORATION □ MAYNARD, MASSACHUSETTS

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KT8/I

TIME-SHARING OPTION FUNCTIONAL DESCRIPTION

The KT8/I Time-Sharing Option provides the additional logic circuits required for use by the PDP-8/I in the TSS/8 Time-Sharing System. Certain configurations of PDP-8/I I/O devices and other options must also be used with the TSS/8 Time-Sharing System. The minimum equipment required for a four-user TSS/8 Time-Sharing System is:

a. PDP-8/I with KT8/I Time-Sharing Option

b. MC8/I-A Memory Extension Control and 8192 Words of Memory

c. RF08 Disk Control

d. RS08 Disk File

e. PT08C Asynchronous Serial Line Interfaces-Full Duplex (Dual Channel) (Four Required)

f. PR8/I High-Speed Tape Reader-300 Characters per Second

g. KE8/I Extended Arithmetic Element (EAE)

h. CAB 8/IA Option Cabinet

The TSS/8 Time-Sharing System permits up to 16 users to operate their individual programs in the PDP-8/I in an apparently simultaneous manner. Operation and reaction time of some I/O devices and of human operators is slow compared to the speed of the central processor. Time sharing allows the central processor to proceed to other tasks rather than wait for slow operations of I/O devices and human operators. In this way the processor can deal with many users and make it appear as if each had full use of the processor. Each user's program is executed for only a fraction of a second at a time, and the different programs are interspersed without interfering with each other and without noticeable delays in the responses to each user.

TSS/8 MONITOR PROGRAM

Time sharing of the PDP-8/I central processor among a group of users is controlled by a group of subprograms called the TSS/8 Monitor which coordinates the operation of various I/O devices, allocates central processor time and services to the users, and controls user access to the central processor.

User programs are usually stored in disk memory and are transferred into core memory to be run. Activation of the user programs is handled by a sequential-loop algorithm under the control of the TSS/8 Monitor. The user program is allowed to run for a fixed period of time, and is then stopped. The contents of the program counter and the various registers are stored at the time execution is stopped; the program is returned to disk storage; and the next user program is read into core memory for processing.

User programs are terminated by the TSS/8 Monitor for various reasons other than the expiration of their allotted time period. They are terminated when an output buffer is filled, when an input is requested and the input buffer is not filled, and for certain other conditions. Thus, central processor time is not wasted waiting for comparatively slow I/O devices.

User programs are not allowed to perform HLT, OSR, or IOT instructions in the usual manner because normal processing of these instructions

would disrupt the operation of the central processor or interfere with the operation of I/O devices shared with other users. When one of these instructions appears in a user program, a user interrupt takes place and the TSS/8 Monitor takes control of the central processor. Three instructions are added by the KT8/I to permit the TSS/8 Monitor to process user interrupts caused by HLT, OSR, or IOT instructions.

KT8/I PROGRAM INSTRUCTIONS

The KT8/I uses three instructions to permit the TSS/8 Monitor to handle user interrupts and to control the user interrupt logic circuits. These instructions are listed with their octal codes and descriptions in Table 1.

executive mode and the TSS/8 Monitor is in control of the central processor. The three added instructions are used by the TSS/8 Monitor only in the executive mode and are never used by a user program. If a user program attempted to use one of these instructions, execution of the instruction would be blocked and a user interrupt would result because they are IOT (octal code 6XXX) instructions. The KT8/I option adds the necessary hardware to the PDP-8/I to implement these three instructions.

HARDWARE

The backplane wiring necessary for the KT8/I Time-Sharing Option is included in the PDP-8/I computers with basic frame serial numbers greater than 996.

Table 1
KT8/I Program Instructions

Mnemonic Code	Octal Code	Description
CINT	6204	Clear user interrupt. Resets the user interrupt (UINT) flip-flop to the 0 state.
SINT	6254	Skip on user interrupt. When the user interrupt (UINT) flip-flop is in the 1 state, sets the user skip flag (USF) flip-flop to the 1 state and causes the program to skip the next instruction.
CUF	6264 6274	Change user flag. Changes the user buffer (UB) flip-flop to the state of MB 08 of the CUF instruction word. Inhibits processor interrupts until the next JMP or JMS instruction. Generation of IB → IF during the next JMP or JMS instuction transfers the state of UB to the user field (UF) flip-flop.

The KT8/I operates in two modes as denoted by the user flag (UF) flip-flop. When the UF flip-flop is in the logic 1 state, operation is in the user mode and a user program is running in the central processor. When the UF flip-flop is in the logic 0 state, operation is in the

To implement the KT8/I option in PDP-8/I computers with earlier serial numbers, a new logic frame must be purchased and installed. Installation of the logic frame must be performed by DEC Field Service personnel.

Four modules and one module that is shared with the PDP-8/I and the extended memory option are required for the logic circuits of the KT8/I Time-Sharing Option. These modules are shown installed in the PDP-8/I in Figure 1 and are listed in Table 2.

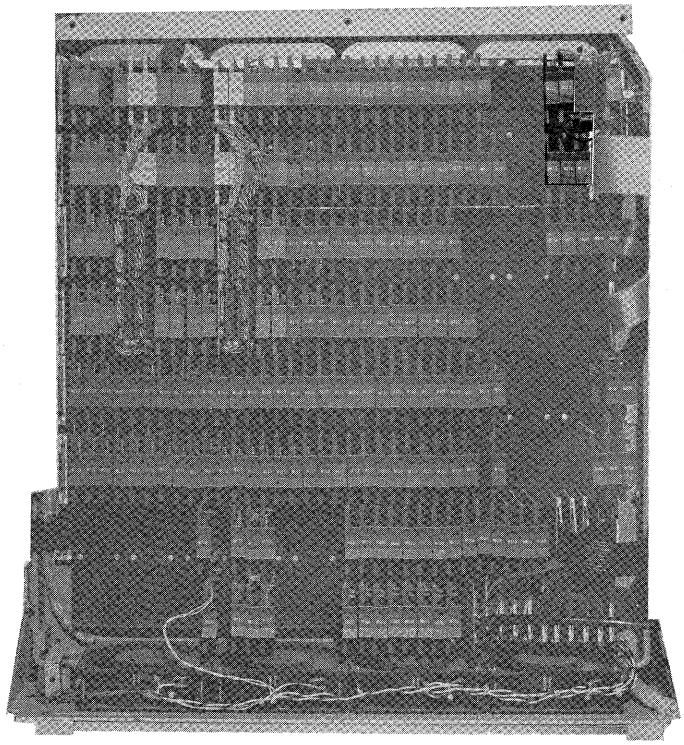


Figure 1 PDP-8/I with KT8/I Modules Installed

Table 2
KT8/I Modules

Quantity	Module Type No.	Use	Location	
			Row	Slot
1	M216	Flip-Flops	B	05
3	M113	NAND Gates	A	05
			A	06*
			B	06
1	M115	NAND Gates	B	04

*This module is shared with the PDP-8/I and the extended memory option.

GENERAL LOGIC DESCRIPTION

Types of Interrupts

The PDP-8/I central processor operates in the executive mode (UF(0) high) so that the TSS/8 Monitor can perform the necessary housekeeping and service routines, or in the user mode (UF(1) high) so that an individual user program can use the central processor to perform its programmed tasks. Either mode of operation is subject to program interrupts which are handled by the interrupt logic of the central processor.

In the TSS/8 Time-Sharing System, program interrupts are caused by I/O devices, the real-time clock, and the user program.

Interrupts caused by I/O devices are similar to the I/O interrupts that occur with a single-user PDP-8/I and are processed in the same way.

The real-time clock, a required option for the time-sharing system, also causes interrupts. A real-time clock interrupt occurs about every 17 ms while the user program is running, so that the executive mode can be used for the TSS/8 Monitor to perform the housekeeping routines required for management of the time-sharing system. For instance, on every third 17 ms interrupt the teletype lines are scanned. Real-time interrupts also terminate the user program operational period of approximately 200 ms.

When a user program is running (user mode), programming of an HLT, OSR, or IOT instruction causes an interrupt. The user interrupts are necessary to prevent a user program from disrupting the operation of the central processor or from interfering with the operation of I/O devices shared with other users.

A simplified block diagram of the logic circuits that generate an interrupt when an HLT, OSR, or IOT is programmed in the user mode is shown in Figure 2. The 1-side output of the UF flip-flop is applied to an AND gate; the other input to the AND gate is a signal resulting from a decoded HLT, OSR, or IOT instruction. Output of the AND gate sets the UINT flip-flop when UF(1) is high and an HLT, OSR, or IOT instruction is decoded. When UINT is set, the signal $\overline{\text{UINT}}$ goes low and provides a signal to the interrupt bus of the central processor.

Processing Interrupts

The I/O, real-time clock, or user program interrupts cause the following sequence of operations:

a. The state of the user flag (UF) flip-flop is transferred to the save user flag (SUF) flip-flop (refer to Figure 2) by signal IF → SF.

b. The user flag (UF) and user buffer (UB) flip-flops are cleared by the $\overline{\text{CLEAR}}$ IF signal. Operation is changed to executive mode (UF (0) high) if operation was in the user mode.

c. The interrupt logic of the PDP-8/I causes an automatic JMS 0000 instruction.

d. One of the first instructions in the subroutine is a read interrupt buffer (RIB) which transfers the state of the SUF onto the $\overline{\text{ME 05}}$ line so that the SUF bit can be stored in memory along with the content of the save field register.

e. The subroutine checks for the cause of the interrupt.

f. One of the final instructions in the subroutine is a turn interrupt on (ION) which re-enables the interrupt logic.

If the interrupt is caused by an I/O device, a jump is made to a subroutine which services the I/O device.

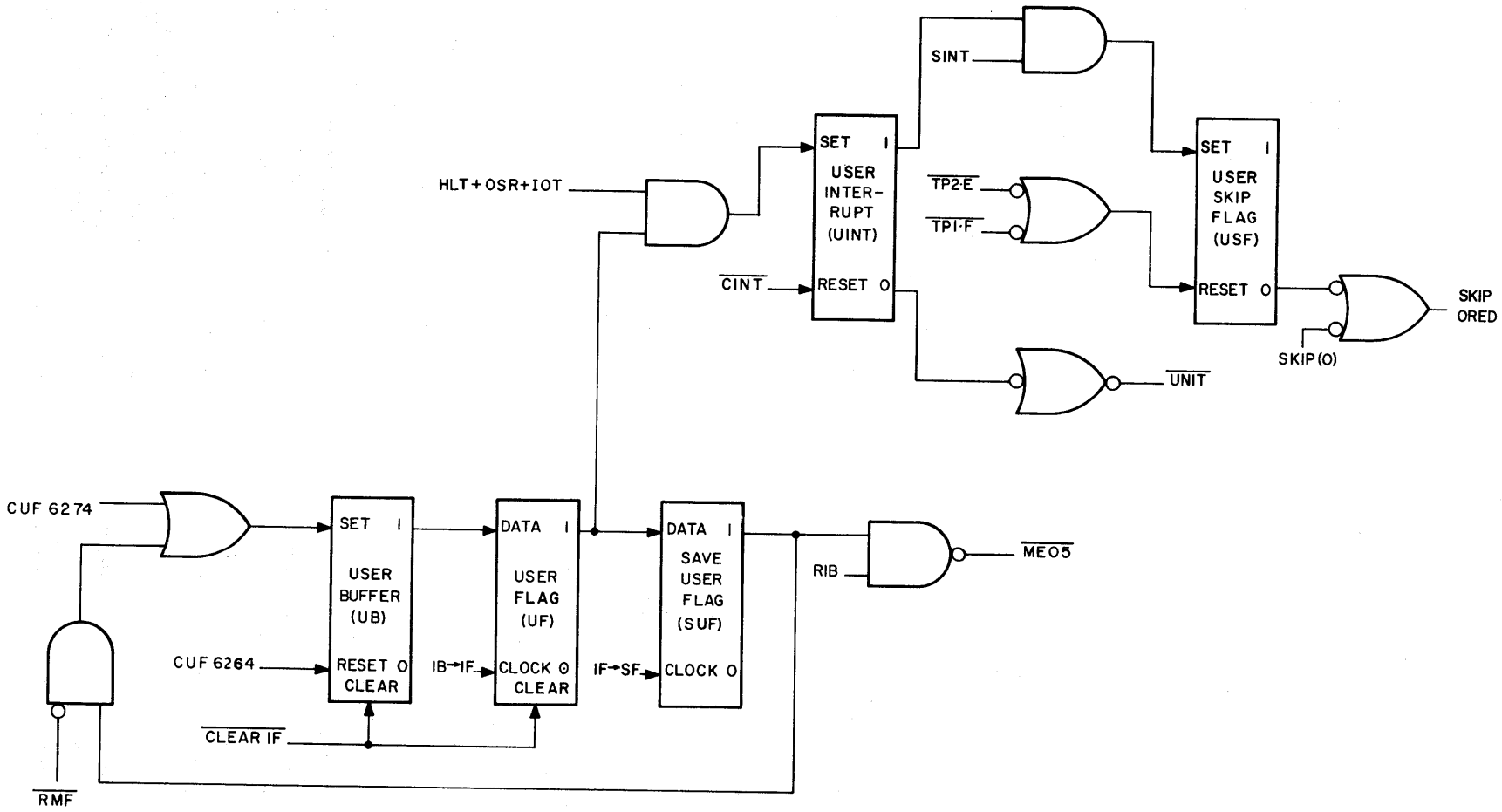


Figure 2 KT8/I Simplified Block Diagram

If the interrupt is caused by the real-time clock, a jump is made to a subroutine that checks the timing pulse count. An appropriate subroutine is used for the housekeeping functions scheduled for that timing count. If the timing count designates the end of the user program running period, the user program queue is checked for availability of another user program.

User Program Interrupts

To check whether the interrupt is caused by the user program, a skip on user interrupt (SINT) instruction is used (refer to Figure 2). The 1 side of UINT is AND gated with signal SINT so that the user skip flag (USF) is set when UINT is set and a skip on user interrupt (SINT) instruction is decoded. With USF set, the SKIP ORED signal is high and the next program step is skipped. The USF is reset by signal $\overline{TP2 \cdot E}$ or $\overline{TP1 \cdot F}$ during the execute or fetch cycle of the next instruction after the skip instruction. The skip causes the program to enter a subroutine that services the interrupt. One of the first instructions in the subroutine is a clear user interrupt (CINT) which clears the user interrupt (UINT) flip-flop.

Performance of any HLT, OSR or IOT instruction in the user program is automatically blocked by the KT8/I logic circuits and the TSS/8 Monitor takes program control. For an HLT instruction, the TSS/8 Monitor halts the user program and checks the user program queue for the next user program available to be run. For an OSR instruction, the content of the core location which has been designated as the switch register for this user program is processed under TSS/8 Monitor control in accordance with the switch register instruction in the user program.

For an IOT instruction, the TSS/8 Monitor takes a different course of action for the various IOT instructions. A complete list of IOT instructions available to the user of the TSS/8 is provided in Appendix C of the TSS/8 Monitor Manual (DEC-T8-MRFA-D). In general, the TSS/8 Monitor handles the processing of the IOT instruction in the executive mode in such a manner that I/O devices shared by other users are not interfered with, no central processor time is wasted waiting for a slow I/O device, and the user program accomplishes the I/O function.

Use of RMF Instruction

In some cases where the TSS/8 Monitor can process an interrupt quickly and without interfering with the save field register, the SUF bit is not transferred to memory by use of a RIB instruction. When interrupt processing is completed, the instruction field register and the user flag (UF) are restored by use of a restore memory field (RMF) instruction. Signal $\overline{RMF}$ transfers the bit in SUF into UB. The TSS/8 Monitor then uses a JMP instruction to return to the appropriate program address. Signal IB → IF is generated when the JMP instruction is used and transfers the bit in UB into UF. The program then continues in either the executive or user mode until the next interrupt.

Return Routine

After completion of a subroutine which services an interrupt, a return routine is used to go back to the operating status at the time the interrupt occurred. As part of this return routine, the user field (UF) flip-flop must be restored to the state it was in at the occurrence of the program interrupt.

At the start of the interrupt the UF was transferred to the SUF and from there to the central processor memory via the $\overline{ME\ 05}$ line. Since no hardware provision is made to transfer the SUF bit from the core memory back into the UF logic circuits, the TSS/8 Monitor must check

the status of the SUF bit and then program a change user flag (CUF) instruction to restore the UF. The CUF instruction either clears (6264) the UB or sets (6274) the UB (refer to Figure 2). When the TSS/8 Monitor has restored all registers and memory fields to the status they occupied at the time of the interrupt, a JMP instruction returns to the program address following the address that was interrupted. The JMP instruction causes the generation of signal IB → IF which transfers the UB bit into the UF flip-flop. The program then continues in either the executive or the user mode until the next interrupt.

Flow Diagram

The flow diagram for the KT8/I Fetch cycle of user program instructions is shown in engineering drawing D-FD-KT8-I-2. This diagram shows when the UINT flip-flop is set for an IOT, HLT, or OSR instruction.

When processing an IOT instruction and UF(1) is high, the UINT is set at TP3 time. When processing an OPR instruction in Group 2 (MB 03 = 1 and MB 11 = 0) and UF(1) is high, the UINT is set for two different conditions. An HLT instruction (MB 10 = 1) or an OSR instruction (MB 09 = 1) causes the UINT to be set at TP3 time.

When UINT is set for an IOT, HLT, or OSR instruction, the interrupt bus to the central processor goes high and activates the interrupt logic circuits of the central processor. Operation is changed to the executive mode (UF (0) high) and a JMS 0000 becomes the next program instruction.

DETAILED LOGIC DESCRIPTION

Engineering drawing D-BS-KT8-I-1 is a detailed block schematic of the logic circuits that are added to the PDP-8/I for the KT8/I Time-Sharing Option. The user buffer (UB), the user flag (UF), save user flag (SUF), user interrupt (UINT) and user skip flag (USF) flip-flops with their associated gating circuits are shown on this diagram. The UB, UF, and SUF flip-flops can be considered as 1-bit extensions of the instruction buffer (IB) register, the instruction field (IF) register, and the save field (SF) register, respectively. These registers are part of the extended memory logic and are shown on engineering drawing D-BS-MC8I-0-1, sheets 1 and 2. The signals used to transfer bits among these registers are also used to transfer a bit among the UB, UF, and SUF.

User Buffer

The bits of the instruction word are decoded by the logic gates shown in area B6 and 7 of engineering drawing D-BS-KT8-I-1. Decoding of the octal instruction 6264 (CUF) results in a clock input to the UB flip-flop. Because memory bit 08 is 0, the data input to the UB remains low so that UB is reset. When the instruction word is octal 6274, memory bit 08 is 1 so that the data input to UB is high when the clock input is high and the flip-flop is set.

The UB is cleared by the $\overline{\text{PC LOAD} \cdot \text{SR ENABLE}}$ signal when the LOAD ADD switch on the front panel of the PDP-8/I is used. Clearing of the UB is also accomplished by the $\overline{\text{CLEAR IF}}$ signal which occurs when the content of the IF register of the extended memory unit is transferred to the SF register (D-BS-MC8I-0-1, sheet 1) in preparation for processing an interrupt.

The state of the SUF flip-flop is transferred to the UB flip-flop when the TSS/8 Monitor issues a restore memory field (RMF) instruction. The inverted $\overline{\text{RMF}}$ signal is NAND gated with the EXT GO signal to provide a clock input to UB. Signals SUF (1) and SF ENABLE are combined in a NAND gate to supply the data input of UB

with a signal that transfers the state of SUF to UB.

User Flag

The 1-side output of UB is NAND gated with the KEYLA MFTS 0 signal so that transfer of the bit in UB to the UF is inhibited during a key load address operation. Signal IB → IF, which occurs at TP3 during a JMP or JMS instruction, is used to clock UF and thereby transfer the state of the UB to the UF.

The UF is cleared at the same time the UB is cleared by the CLEAR IF signal. The clearing of the UF and UB by the CLEAR IF signal is done when an interrupt is being processed and the central processor must go into executive mode (UF (0) high). Prior to the clearing of the two flip-flops, the bit in UF is transferred to the save user flag (SUF) flip-flop.

Save User Flag

The 1-side output of UF provides the data input to SUF so that the bit in UF is transferred to SUF when SUF is clocked by signal IF → SR. This signal is the same signal that transfers the contents of the information field register to the save field register (engineering drawing D-BS-MC8I-0-1, sheet 1) of the extended memory logic. Transfer to the SUF is done when the TSS/8 Monitor is processing an interrupt. Signal INT OK is used to generate the LOAD SF signal at TS4 time (engineering drawing D-BS-8I-0-7), and LOAD SF generates signal IF → SF.

The 1-side output of SUF is combined in a NAND gate with RIB, which is high when the read interrupt buffer (RIB) instruction is decoded by the extended memory logic (engineering drawing BS-MC8I-0-1, sheet 2). The RIB instruction therefore reads the bit in SUF into bit 5 of the AC on the ME 05 line which activates the INPUT BUS 05 line in the central processor.

The bit in the SUF flip-flop is transferred to the UB flip-flop when the TSS/8 Monitor issues a restore memory field (RMF) instruction. A description of the logic circuits that accomplish this transfer is provided in the user buffer section.

Signal INITIALIZE clears the SUF during start-up of the system when the power supply reaches the proper level, when power begins to fail, or when the START key is depressed.

User Interrupt

The user interrupt (UINT) flip-flop is shown in area D3 of engineering drawing D-BS-KT8-I-1. Gates located in area DC6 and 7 of this same engineering drawing decode an HLT or OSR instruction and provide an input to a NOR gate. The other input to this NOR gate is provided by signal I - IOT, which is low whenever an IOT instruction (octal code 6XXX) is decoded. The output of the NOR gate is combined in a NAND gate with the 1-side output of UF, and the output of the NAND gate provides the data input to the UINT. The result of this gating is that the UINT is set at TP3 time when the UF is in the 1 state and an HLT, OSR, or IOT instruction is decoded.

When the UINT is set to the 1 state, it remains in this state until a clear user interrupt (CINT) instruction is decoded. A NAND gate in area D4 of engineering drawing D-BS-KT8-I-1 has inputs of CINT and UINT (1) so that the data input to UINT remains high until the NAND gate shown in area C6-7 decodes a CINT instruction and signal CINT goes low. Signal INITIALIZE also clears UINT during start-up of the system when the power supply reaches the proper level, when power begins to fail, or when the START key is depressed.

The UINT signal is generated by a NOR gate that has as inputs the UINT (0) signal and the signal that originally set the UINT flip-flop.

The $\overline{\text{UINT}}$ signal is used, by the logic circuits shown in area A6 on engineering drawing D-BS-8I-0-12, to generate the $\overline{\text{TT INT}}$ signal. These teletype logic circuits provide a signal to the interrupt bus of the central processor. Therefore, whenever the UINT is in the 1 state, the interrupt bus of the central processor is activated.

User Skip Flag

The user skip flag (USF) flip-flop is shown in area D2 of engineering drawing D-BS-KT8-I-1. Gates shown in area B6 of this same engineering drawing are used to decode the skip on user interrupt (SINT) instruction. The output of these gates is combined in a NAND gate with TP3 and UINT (1). Output of the NAND gate provides the set input for USF so that USF is set at TP3 when UINT is in the 1 state and a SINT instruction is decoded.

The clock input of USF is provided by a NOR gate which has signals $\overline{\text{TP2}\cdot\text{E}}$ and $\overline{\text{TP1}\cdot\text{F}}$ as inputs. These input signals are generated by the logic circuits shown in area D2 and 3 of engineering drawing D-BS-8I-0-6. Since the data input is grounded, the SUF is cleared at TP2 of the Execute cycle or at TP1 of the Fetch cycle. Signal $\overline{\text{INITIALIZE}}$ also clears the USF during start-up of the system when the power supply reaches the proper level, when power begins to fail, or when the START key is depressed.

The 0-side output of USF and signal SKIP (0) provide inputs to the NOR gate shown in area D2 of engineering drawing D-BS-KT8-I-1. Output signal SKIP ORED from this gate is used by the logic circuits shown in area B4 of engineering drawing D-BS-8I-0-5 to generate a $\overline{\text{CARRY INSERT}}$ signal. With the $\overline{\text{CARRY INSERT}}$ signal present, the content of the program counter is incremented by one when it is transferred to the memory address register at T4 time of the Fetch cycle with the result that the next program instruction is skipped. Thus, a SINT instruction causes the next program instruction to be skipped when the UINT is in the 1 state.

Instruction Inhibit Logic

Operation of the TSS/8 Time-Sharing System requires that the user program be prevented from interfering with the operation of the central processor and the operation of the I/O devices. Therefore, normal execution of the HLT or the IOT instructions in the user program is inhibited.

Normal execution of an OSR instruction in the user program is also inhibited. This treatment of the OSR instruction is necessary because the various users who are sharing time on the central processor do not have access to the switches on the front panel of the PDP-8/I. Switch register entries are made by use of the Teletype keyboard. The TSS/8 Monitor interprets a properly coded teletype entry as a switch register input and allocates the data to a core location designated as the switch register for the user program being executed. Therefore, an OSR instruction in the user program must be handled in a different manner.

Programming of an HLT, IOT, or OSR instruction by the user program results in the inhibition of normal execution of the instruction and the sending of an interrupt request to the central processor. Operation is changed to the executive mode and the TSS/8 Monitor processes the instruction.

An HLT instruction in the user mode (UF (1) high) causes the UINT flip-flop to be set and the HLT instruction to be inhibited. Blocking of the HLT instruction is accomplished by use of the UF (0) signal as an input to the AND gate which resets the RUN flip-flop for an HLT instruction (engineering drawing D-BS-8I-0-2, sheet 1).

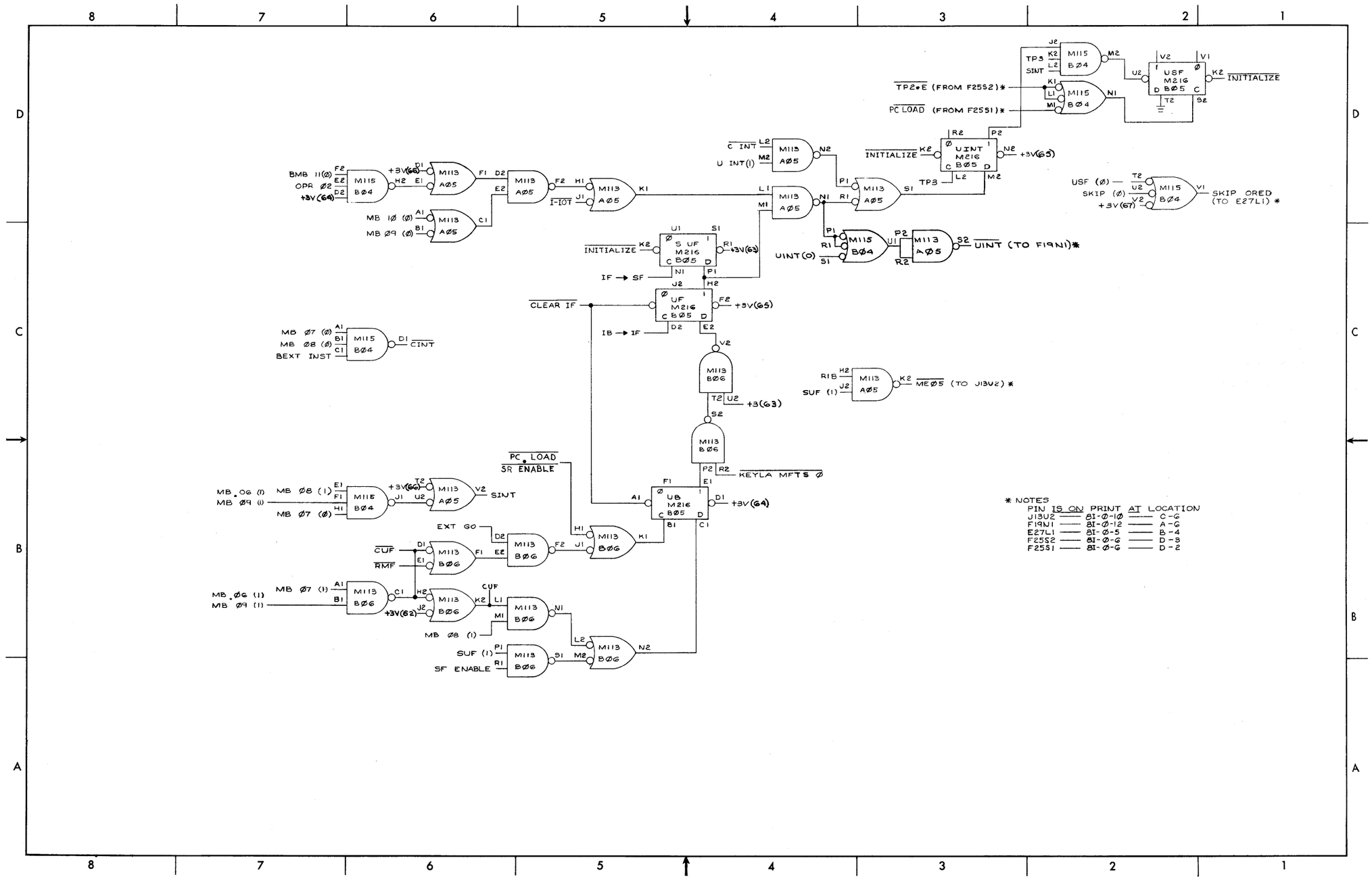
An IOT instruction (octal code 6XXX) in the user mode (UF (1) high) causes the UINT flip-flop to be set and the IOT instruction to be inhibited. Blocking of the IOT instruction is accomplished by use of the UF (0) signal as an input to the NAND gate which decodes the instruction register bits and generates the IOT and $\overline{\text{IOT}}$ signals (engineering drawing D-BS-8I-0-3).

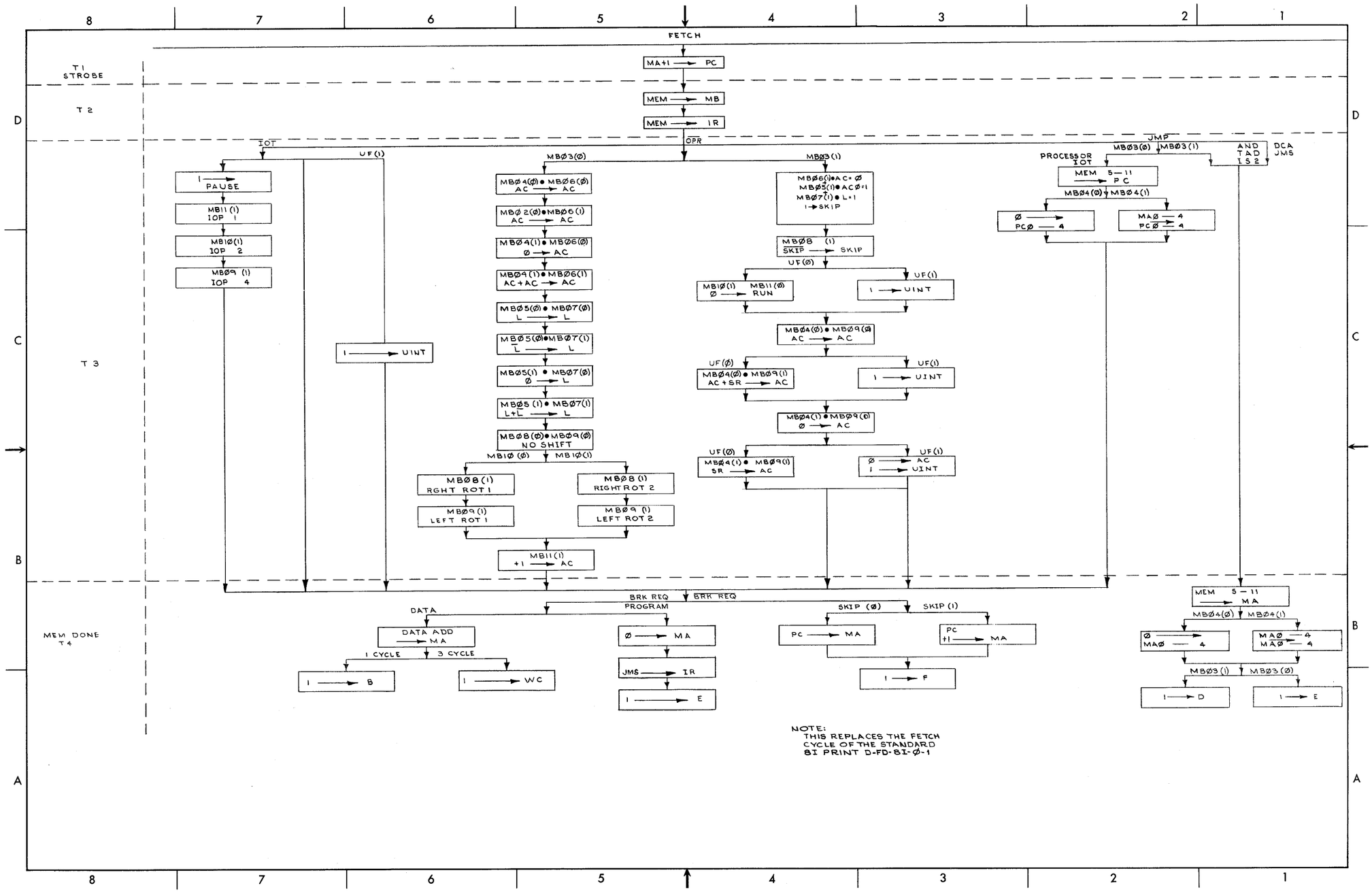
An OSR instruction in the user mode (UF (1) high) causes the UINT flip-flop to be set and the OSR instruction to be inhibited. Execution of the OSR instruction is blocked because the UF (0) signal is NAND gated with signal OSR to generate the SR ENABLE signal (engineering drawing D-BS-8I-0-4).

ENGINEERING DRAWINGS

The engineering drawings for the KT8/I Time-Sharing Option listed below are included in this section. It is also necessary to consult the block schematic diagrams for the Memory Extension Control Option (D-BS-MC8I-0-1, sheets 1 and 2) and for the basic PDP-8/I Computer (D-BS-8I-0-XX series) to follow the logic discussions in this publication.

Drawing Number	Title
D-BS-KT8-I-1	KT8/I Time Sharing Option
D-FD-KT8-I-2	KT8/I Fetch Cycle
A-SP-KT8-I-4	Engineering Specification


BMB 11(Ø)
OPR Ø2
+3V(G4)
MB 1Ø (Ø)
MB Ø9 (Ø)
I-IOT
U INT (I)
C INT
INITIALIZE
TP3
SINT
TP2•E (FROM F2552)*
PC LOAD (FROM F2551)*
USF (Ø)
SKIP (Ø)
+3V(G7)
SKIP ORED (TO E27L1) *
IF → SF
CLEAR IF
IB → IF
MB Ø7 (Ø)
MB Ø8 (Ø)
BEXT INST
CINT
UINT(Ø)
UINT (TO F19N1)*
RIB
SUF (1)
ME Ø5 (TO J13U2) *
+3(G3)
KEYLA MFTS Ø
PC LOAD
SR ENABLE
MB Ø6 (1)
MB Ø9 (1)
MB Ø8 (1)
MB Ø7 (Ø)
SINT
+3V(G4)
EXT GO
CUF
RMF
MB Ø7 (1)
+3V(G2)
SUF (1)
SF ENABLE
* NOTES
PIN IS ON PRINT AT LOCATION
J13U2 —— 8I-Ø-1Ø —— C-6
F19N1 —— 8I-Ø-12 —— A-6
E27L1 —— 8I-Ø-5 —— B-4
F2552 —— 8I-Ø-6 —— D-3
F2551 —— 8I-Ø-6 —— D-2



D-FD-KT8-I-2 KT8/I Fetch Cycle

REVISIONS

REV	DESCRIPTION	CHG NO	ORIG	DATE	APPD BY	DATE
-	ORIGINATED -	8I-00025	-	12/23/68	-	-

Ø.Ø OVERALL DESCRIPTION

The KT8I option converts the PDP-8I for time sharing by:

A. Adding means for interrupt

B. Adding four (4) new IOT's for control

C. Extending by one bit (in the memory extention control type MC8I the instruction buffer (IB), instruction field (IF) and the save field (SF).

1.Ø GENERAL SPECIFICATION

1.1 Opterational Description

The instructions for HLT, OSR and IOT are modified in "user mode" (UF=1) so the normal machine functions are inhibited. The new function (only UF=1) is a means of interrupt for the user. If the program is in "executive mode" (UF=Ø), the normal machine functions for HLT, OSR and IOT are returned to normal. A JMS or JMP transfers the contents of the user buffer (UB) to the user field (UF). Interrupt acknowledge or load address (key) will transfer the user field (UF) to save user field (SUF) and clear the UF and UB.

Restore memory field (RMF 6244_8) loads the user buffer (UB) with the contents of same user field (SUF).

1.2 Packaging

The KT8I option is part of the PDP-8I main framing wiring.

1.3 Environmental Specifications

1.3.1 Operating temperature 0^{o} - $130^{o}F$

1.3.2 Noise Immunity 1 volt

1.3.3 Power comsumption for the KT8I option modules are:

+5 volts DC at 169 ma.

2.Ø SPECIFICATION OF VENDOR-SUPPLIED EQUIPMENT

None

3.Ø PROGRAMMING

3.1 IOT codes, mnemonics and description

MNEMONIC	OCTAL CODES	DESCRIPTION
CUF (Change User Field)	6264	Sets the User Buffer flip-flop to a zero (state of MB8). The following JMP or JMS will transfer the state of UB to the user field. EXECUTION TIME: 1.5 microsec.
CUD (Change User Field)	6274	Sets the User Buffer flip-flop to a one (state of MB8). The following JMP or JMS will transfer the state of UB to the user field EXECUTION TIME: 1.5 microsec.
CINT (Clear Interrupt	62Ø4	Resets the User Interrupt flip flop. EXECUTION TIME: 1.5 microsec.
SINT (Skip on Interrupt)	6254	Causes the program to skip if the User Interrupt flip-flop is in the ONE state. EXECUTION TIME: 1.5 microsec.

3.2 Test and/or Diagnostic

There are two (2) tests available for the KT8I options. MAINDEC T8-D8A (KTØ8 Test) and MAINDEC T8-D8B (Systems Test

3.2.1 Requirements and procedures for MAINDEC T8-D8A (KTØ8 test).

3.2.1.1 Requirements

A. DF32 Disk

B. Standard PDP-8I computer with KT8I time shared option and type MC8I memory control.

3.2.1.2 Procedure

A. Load MAINDEC T8-D8A using standard binary loader

B. Starting address is 200_8

Note: During operation the switch register should never equal zero and "JUMP to self" is used for error conditions.

C. The program should halt at $PC212_8$ and $PC220_8$. Press continue in each case. The program will run for about five minutes and come to rest (JUMP to self) at $PC753_8$.
Program listing and write-up should be consulted if more detail is required.

3.2.2 Requirements and Procedures

MAINDEC T8-D8B (System Test)

3.2.3 Requirements

Being developed.