PRISM

ARCHITECTURE

DECwest Engineering

Rev:2 / January 1986 #1

PRISM:

Parallel
Reduced
Instruction
Set
Machine

DECwest Engineering

Rev:2 / January 1986 #2

Is PRISM "RISC"?

- RISC = Reduced Instruction Set Computer
  - IBM 801
  - Berkeley
  - Titan, Safe, Cascade...
- Small Instruction Set
- Instructions in Hardware
- "RISC" compared to VAX?

But...
PRISM isn't RISC!

PRISM is:

- **Parallel Architecture**
- **Vectors**
- **Some "RISC" Concepts**
- **Some "CISC" Concepts**
- **Designed for PERFORMANCE**

PRISM ARCHITECTURAL GOALS

- High (Absolute) Performance
- 2:1 (or better) Cost/Performance
- VAX Compatibility
- VAX Extension Architecture for 1990's

DECwest Engineering

Rev:2 / January 1986 #5

Why Not Build A Faster VAX?

- Complex (microcoded) instruction set
- Variable length instructions
- Many addressing modes (good & bad)
- 512 byte page size
- Autoincrement & Autodecrement
- Condition codes force synchronization
- Lots of unused functionality

DECwest Engineering

Rev:2 / January 1986 #6

PRISM
ARCHITECTURE OVERVIEW

- 32-bit architecture
- 32-bit virtual address space
- 45-bit physical address space
- VAX compatible memory addressing
- VAX compatible data types
- Scalar and vector processing
- Symmetric multiprocessing

DECwest Engineering
Rev:2 / January 1986 #7

SCALAR PROCESSING

- 64 32-bit registers
- 8-, 16-, 32-bit integers/logicals
- 32- and 64-bit F_ and G_Floating
- Parallel instruction execution
- Comprehensive, yet simple, instruction set
- Load/Store memory referencing

VECTOR PROCESSING

- 16 vector registers
- 64 elements per vector register
- 64-bits per vector element
- 32-bit integer/logicals
- 32- and 64-bit F_ and G_Floating
- Single instruction processes entire vector register
- Similar to Cray-2 vector functionality

MEMORY MANAGEMENT

- 32-bit virtual address space
- Basis for relocation, protection and paging
- Execute protection for proprietary code
- 8KB page size for added TB efficiency

DECwest Engineering

Rev:2 / January 1986 #10

PRISM ADVANTAGES

- Fixed length instructions
- Lots of registers
- Parallel execution; out-of-order completion
- No (synchronous) condition codes
- No compound instructions
- No microcode required
- Large pages

CRYSTAL

HARDWARE SUMMARY

DECwest Engineering

Rev:2 / January 1986 #1

Crystal Processor

Basics:

- PRISM Architecture
- Air-Cooled, ECL Multiprocessor (1-4)
- Scalar with vector option(s)

Performance:

- 3X equivalent VAX per scalar unit
- 100 + MFLOPS (Peak) per vector option
- Memory Size = 128 to 512 MBytes
- I/O Bandwidth > 50 MBytes/sec

Transfer Costs:

	Proc	Memory	MLP	TC	Markup
Entry Kernel	2	128 MB	$ 1465K	$ 169K	8.7X
Max Kernel	4	512 MB	$ 3733K	$ 451K	8.3X

DECwest Engineering

Rev:2 / January 1986 #2

Crystal Scalar Unit

Performance through both fast clock cycle and parallelism

- High speed ECL gate arrays - 15nS cycle
- Retire an instruction each cycle
- Four independent function units
- Fully pipelined multiply and add
- Separate instruction and data caches
- Data cache is writeback

DECwest Engineering

Rev:2 / January 1986 #3

Crystal Vector Option

Architecture and fast clock cycle provide very high throughput

- Sixteen multiported vector registers
- Four autonomous function units
- Fully pipelined multiply and add
- 132 Mflops peak performance
- 2 board addition to Scalar processor

DECwest Engineering

Rev:2 / January 1986 #4

Crystal Memory System

Parallelism used to achieve very high performance

- 1-2+ Gigabytes/Second
- MultiLevel cache hierarchy
- Main memory is 32 way interleaved
- Memory size 128 to 512 MBytes

Crystal I/O System

Multiple Channels and Independent Processors used to achieve high bandwidth

- VAXBI allows standard DEC devices
- I/O Processors off-load main CPU
- VAX as IOP allows BCA
- Memory on IOP maximizes BI bandwidth
- Eight VAXBIs provide 64Mbytes/sec

DECwest Engineering
Rev:2 / January 1986 #6

PRISM/VMS

Software Summary

DECwest Engineering

Rev:2 / January 1986 #1

PRISM/VMS GOALS

- Quality
- Robustness, Extendability, and Maintainability
- New Functionality
- VMS Compatibility
- Schedule
- Performance

SOFTWARE SUMMARY

- Very similar to VAX/VMS
- ULTRIX
- Cluster Support
- Symmetrical MP
- Vector Support
- Multitasking

DECwest Engineering

Rev:2 / January 1986 #3

SOFTWARE SUMMARY - CONT.

- PILLAR Systems Implementation Language

- Layered Languages:
  - Vectorizing FORTRAN
  - BLISS
  - Pascal
  - C

VMS COMPATIBILITY

At user interfaces and at VAX/VMS interfaces:

- **System services via compatibility layer**
- **Disk and Magtape structures**
- **DCL and utilities**
- **DECnet and remote terminal support**
- **Clusters**
- **Languages, RTL, and debugger**
- **Layered Products**

DECwest Engineering

Rev:2 / January 1986 #5

PRISM COMPETITION

SUMMARY

DECwest Engineering

Rev:2 / January 1986 #1

Competition

- IBM
- Technology Leaders
- Others

High Technology Companies

- Convex (C-1)
- Alliant (FX/1 and FX/8)
- Scientific Computer Systems (SCS)
- Elxsi (System 6400)
- Floating Point Systems (FPS-164 and FPS-264)
- Market Share for These & Other High Technology Companies
  - . 4% FY85 ($625K-1.6M Priceband)
  - . 2% FY85 ($1.6M + Priceband)

Product Comparison Summary

	Crystal	IBM	Convex	Alliant	Amdahl	Cray
Model #	1-4 CPUs	3090 200&400	C-1	FX/8	5890 300&600	2
# Proc	1-4	2,4	5	1-8	2,4	4
VUPs	30-100	21-38	10	3.5-26	30-54	120*
Cost per VUP	$20K	$183K-$188K	$52K	$39K	$170K-$172K	$147K*
MFLOPS	100+ -200+	100 -200	60	94		1600
System Price	$571K-$2.15M	$3.9M-$7.2M	$515K	$270K-$1.0M	$5.1M-$9.3M	$17.6M
VP	Yes	Yes**	Yes	Yes	No	Yes

* Estimated

** Attached Vector Processor

Please note: Crystal systems (which FRS in FY89) are compared to currently shipping competitive systems.

DECwest Engineering

Rev:2 / January 1986 #4

Alliant FX/8

- Price/Performance
  - . 3.5-26 VUPs - $39K per VUP (1-8 Processors)
  - . 94 MFLOPS
  - . $270K-1.0M Systems
- 1-8 Processors
- Vector Processing
- Compiler Technology (Decomposing, Vectorizing)
- Full Fortran Support for Vector Hardware Parallelism

DECwest Engineering

Rev:2 / January 1986 #5

Crystal and Alliant Product Comparisons

	Crystal	Alliant
# of Processors	1-4	1-8*
Processor Bits	32	32/64
Cycle Time	15ns	170ns
Cache	64-256K	64-128K
System Memory	64-512MB	8-64MB
Memory Speed	800MB	188MB
I/O Architecture	IOP	IOP
Vector Processor	Yes	Yes

*1-8 Computational and 12 Interactive Processors

DECwest Engineering

Rev:2 / January 1986 #6

Convex C-1

- Price/Performance
  - . 10 VUPs - $52K per VUP
  - . 60 MFLOPS
  - . Entry System $515K
- 5 Processors
- Vector Processing

Crystal and Convex Product Comparisons

	Crystal	Convex
# of Processors	1-4	5*
Processor Bits	32	32/64
Cycle Time	15ns	50ns
Cache	64-256K	64K
System Memory	64-512MB	4-128MB
Memory Speed	800MB	80MB
I/O Architecture	IOP	IOP
I/O Bandwidth	64-100MB	80MB
Vector Processor	Yes	Yes

* With True Parallelism

DECwest Engineering

Rev:2 / January 1986 #8

Cray-1 and 2

- Cray-1

  . Entry System $8.8M
  . 250 MFLOPS
  . 64 Processor Bits
  . 12.5ns Cycle Time
  . 24 Channels

- Cray-2

  . 4 Processors
  . Entry System $17.6M
  . 1600 MFLOPS
  . 64 Processor Bits
  . 4.1ns Cycle Time
  . 40 Channels

Crystal and IBM Product Comparisons

	Crystal	IBM 3090
# of Processors	1-4	2,4
Processor Bits	32	32
Cycle Time	15ns	18.5ns
Cache	64-256K	64-256K
System Memory	64-512MB	64-256MB
I/O Architecture	IOP	Channels
I/O Bandwidth	64-100MB	96-288MB
Vector Processor	Yes	Yes

DECwest Engineering

Rev:2 / January 1986 #10

MAKING A SUCCESS

OF PRISM

DECwest Engineering

January 16, 1986 #1

PRODUCT POSITIONING

- MARKET
  - High performance
  - Scientific computation
  - Engineering
  - Research

- With AQUARIUS
  - Crystal = high end scientific, computational
  - Aquarius = high end commercial, MIS

- With ARGONAUT
  - Dual processor entry above Argonaut
  - Argonaut = mid-range VAX processor

CONCERNS

- Software schedules tight
- Too much (?) to do now
- FY89 will be here tomorrow
- Software will be gating item

HOW DO WE SUCCEED? - CONT.

- Deliver minimal, but key layered software:
  - Best Vectorizing FORTRAN (period)
  - Supporting tools (LSE, MMS, CMS, PCS, etc.)
  - Sell performance - use the iron!

HOW DO WE SUCCEED?

- Keep our focus narrow:
  - Scientific computing
  - Member of VAX family
  - Top Fortune companies

HOW DO WE SUCCEED? - CONT.

- Catch up with VAX over several years
  - Schedule layered product introductions
  - Complementary offerings (product families)